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Kingsley A. Ogudo
Diethelm Schmieder
Daniel Foty
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Kingsley A. Ogudo
Diethelm Schmieder
Tshwane University of Technology
Department of Electrical Engineering
Laboratory for Innovative Electronic Systems
P.O. Box X680, Pretoria 0001, South Africa
E-mail: schmiederd@tut.ac.za

Daniel Foty
Gilgamesh Associates
LLC, 452 Black Mountain Road
Fletcher, Vermont 05444

Lukas W. Snyman
Tshwane University of Technology
Department of Electrical Engineering
Laboratory for Innovative Electronic Systems
P.O. Box X680, Pretoria 0001, South Africa

Abstract. This paper analyzes the optical propagation and refraction phenomena in various complementary metal–oxide–semiconductor (CMOS) structures at 750 nm wavelength. Operation at these wavelengths offers the potential realizations of small microphotonic systems and micro-opto-electro-mechanical systems (MOEMS) in CMOS integrated circuitry, since Si-based optical sources, waveguides, and silicon (Si) detectors can all be integrated on a single chip. It could also increase the optical coupling efficiencies to external optical fibers. With the help of Monte Carlo and RSoft BeamPROP simulations, we demonstrate achievements with regard to optimizing vertical emission, focusing, refraction, splitting and wave guiding in 0.35 to 1.2 μm CMOS technology at 750 nm wavelength. The material properties, refractive indices, and thicknesses of various CMOS over-layers were incorporated in the simulations and analyses. The analyses show that both Si nitride and Si oxi-nitride offer good viability for developing such waveguides. Effective single-mode wave-guiding with calculated loss characteristics of 0.65 dB $\cdot$ cm^{-1}, with modal dispersion characteristics of less than 0.2 ps $\cdot$ cm^{-1} and with a bandwidth-length product of higher than 100 GHz-cm seems possible. A first iteration realization of an optical link is demonstrated, utilizing specially designed avalanche-based Si-LEDs and a specially designed first iteration CMOS waveguide. Potential applications of avalanche-based Si LEDs into microphotonic systems and MOEMS are furthermore proposed and highlighted.
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1 Introduction

Currently, optical communications and opto-electronic integrated circuits are realized by utilizing "III-V" group semiconductors, such as gallium arsenide and associated compounds. They form the basis of a mature and quite complex technology. A deficiency is that these technologies cannot be integrated into silicon (Si) and mainstream complementary metal–oxide–semiconductor (CMOS) integrated circuit technology with ease.

A series of viable Si light-emitting technologies have recently become available that enable the integration of light sources directly into Si CMOS technology.[1,2] The creation of large-scale opto-electronic integrated circuits and optical data "highways" in CMOS integrated circuitry utilizing Si CMOS compounds have been envisioned and hold much promise.[3–8] The latest attempts for realizing optoelectronic systems in CMOS technology have until now mainly been focused utilizing wavelengths at 1550 nm,[9–11] mainly because of the ease of design and fabrication of waveguides in this regime. However, no effective optical sources and Si detectors are available at this wavelength.

If optical source, detector, waveguides, and sensors could be realized on the same CMOS chip at, say, 750 nm wavelength, various on-chip-based microphotonic systems can be realized. Achieving these goals can lead to diverse low-cost "all-silicon" opto-electronic systems, which will be the "smarter" and more "intelligent" CMOS chips of the future. These systems could lead to new products for especially the medical and bio world. Such a new field could be appropriately named "Si CMOS photonic microsystems." These systems also do not require ultrahigh frequency bandwidths and the emission powers of these Si light-emitting diodes (LEDs) may be sufficient to sustain the operation of such systems. This can lead to many new products and open up new markets.

The main objective of our research was, therefore, to directly integrate the sources and detectors for optical sensors on chip. This would have benefits in terms of cost reduction, miniaturization, the simplification of packaging requirements and perhaps also in total power requirements.

Substantial progress has been made in the field of Si $p-n$ junctions emitting visible light when operating in reverse breakdown avalanche mode.[12–18] Recently, Si CMOS light-emitting sources appeared with much higher efficiencies by

implementing two and three junction Si CMOS injection-avalanche LEDs that emit at 450 to 750 nm.[19,20] They can be integrated with ease in standard CMOS circuits. Various prototypes have been realized. Their operating voltage (8 V), and current (80 μA to 1 mA) are low. They emit from an area of 1×1 μm between 10 and 100 nW. The internal light emission levels are much higher. A particularly promising technology that uses defect and surface-assisted transitions in these types of LEDs has recently been identified and developed by our specific group.[20–22]

Our Si avalanche-based Si LEDs operate optimally at 650 to 850 nm. Although the optical emission power of Si avalanche LEDs is low, they can reach modulation speeds into the GHz range. Since Si LEDs and Si detectors are both available and can be integrated with relative ease into CMOS technology, the most challenging part of following this route is, hence, to develop appropriate CMOS waveguide technology in this wavelength regime in CMOS integrated circuitry.

The purpose of this paper is, then, (1), to present some detailed simulation results for realization of microphotonic structures in 1.2 and 0.35 μm CMOS integrated circuitry at mainly 750 nm operating wavelengths; (2) to demonstrate the possible performance of CMOS waveguides at 750 nm; (3) to demonstrate a realized first iteration optical link in Si-CMOS integrated circuitry at 650 nm; and (4) to propose some first iteration CMOS-based microphotonic systems and micro-opto-electro-mechanical systems (MOEMS) applications.

2 Optical Properties of CMOS Integrated Circuit Structures

Figure 1 shows a typical CMOS integrated circuit structure using 1.2-μm field oxide-based technology. Important

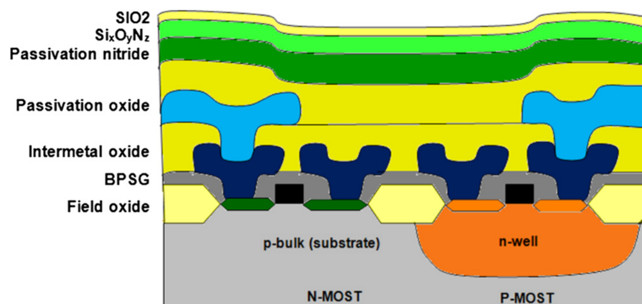

Fig. 1 Typical layers and structures used in CMOS integrated circuits.

features are the transparency of some of the over-layers, such as the field oxide layer, the inter-metallic oxide layers, and the Si nitride passivation layer between 450 and 750 nm wavelengths.[23,24] Other transparent layers such as Si oxi-nitride and Si dioxide can be added as further over-layers.[25–27] The optical transparency of the different layers varies slightly. The dimensions and optical variables as associated with above 0.35 μm CMOS integrated circuit technology are presented in Table 1. The advantage of using this type of technology for microphotonic systems is that the field oxide introduces curvatures into the over-layers that are beneficial for generating microphotonic structures.

The below 0.35 μm CMOS technology is in principle similar, except that the Si field oxide layer is thinner (250 nm) and a planarization process is used after transistor fabrication in order to accommodate a higher number of metal over-layers. The transparency of Si is poor, while the transparency of the field oxide layer is excellent. Si nitride and Si oxi-nitride are transparent for wavelengths longer than 600 nm.[25–27] This is substantially lower than the absorption edge of Si, which lies at 1100 nm. If Si LEDs and Si $p-n$ detectors are used, Si CMOS technology does not have to rely on III-V or Si–Ge technology. In particular this technology utilizes trench isolation technology that can be used for generating in-line opto-couplers and waveguides to even below the Si substrate-overlayer interface.

3 Si CMOS Avalanche LEDs

Si avalanche light-emitting devices in the 450 to 650 nm regimes have been in use for a long time.[12–18] The fabrication of these devices is high-temperature compatible and can be used in standard Si designs. CMOS-compatible avalanche Si LEDs (Si CMOS Av LEDs) have emerged since the early 1990s. Kramer and Zeits[28] were the first to propose the utilization of Si Av LEDs inside CMOS technology. They first illustrated the potential of this technology. Snyman et al., have realized a series of light-emitting devices in standard CMOS technology, such as micro displays and electro-optical interfaces with higher emission efficiencies and higher emission radiances (intensities).[19–21] Particularly promising results have been obtained regarding efficiency and intensity, when a combination of current density confinement, surface layer engineering, and injection of additional carriers of opposite-charge density into the avalanching junction, were implemented.[19] These devices showed three orders of increase in optical output as compared with previous similar work. However, increases in efficiency seemed to be

Table 1 Optical Properties of CMOS ICs at 750 nm.

Component	Thickness (μm)	Refractive index	Absorption coefficient/ transparency per wavelength	State
Si substrate	1 μm	3.76	Transparent above 1100 nm	Crystalline solid
Si field oxide	1 μm	1.45	Transparent above 400 nm	Fused solid
Si plasma oxide	0.9 μm	1.48	0.4–0.2 for ≥400 nm	RF deposited plasma
Si nitride	0.9 μm	2.00	Transparent above 600 nm	RF deposited plasma
Air	Infinite	1.00	Transparent for 400 to 1500 nm	Gas phase

compromised by higher total device currents because of loss of injected carriers, which do not interact with avalanching carriers.

Latest analyses of the work of Kramer et al.[28] and Snyman et al.,[20] shows that longer wavelength emissions up to 750 nm can be achieved by focusing on the electron relaxation techniques in the purer n-side of the Si $p-n$ avalanching junctions. This development has a very important implication. The spectral radiance of this device compares extremely well with the spectral detectivity of the Si reach through avalanche photo detector (RAPD) technology. A particularly good match is obtained between the emission spectrum of this device and the absorption spectrum, which can be detected with an RAPD. More information about the design and performance aspects of our latest E-field and momentum shift assisted 750 nm Si LEDs can be found from Snyman and Bellotti.[20] By controlling the defect density in this device, one can favor either the 650 or 750 nm emissions. Total emission intensities of up to 1 μW per 5 μm^2 area at the Si-SiO_2 interface have recently been observed.

Figure 2 shows a design of a top-down as well as cross-section layout of a Si CMOS and avalanche operation-based LED. The LED consists of an n^+ bar placed opposite to two p^+ bars and diagonally away from the n^+ bar. All were embedded in a p-well containing 2×10^{16} ions. The n^+ and p^+ regions define the peripheries of the SiO_2 field oxide layer and define the center SiO_2 field oxide layer. Upon biasing the structure with positive bias voltage +V on the n^+ and negative bias voltage −V on the p^+ region, the depletion region extends from the n^+ edge facing the p^+ region in the SiO_2 field oxide layer.

The intensity of the emitted light was approximately 1 nW per micron length at an operating voltage of 15 V. A current of 80 μA to 1 mA was emitted between 450 and 750 nm with a tail reaching deep into the near infrared region (Fig. 3).

Si avalanche-based LEDs can be integrated into CMOS circuits with ease, and offer the following advantages:

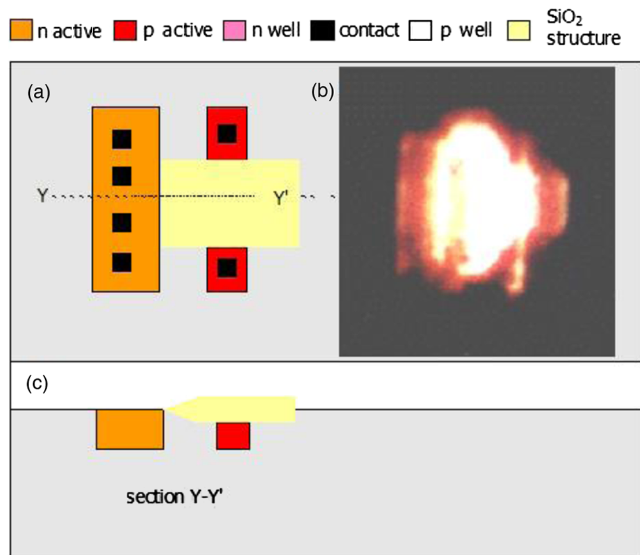

Fig. 2 Si LED integrated in CMOS integrated circuit technology as an optical source.

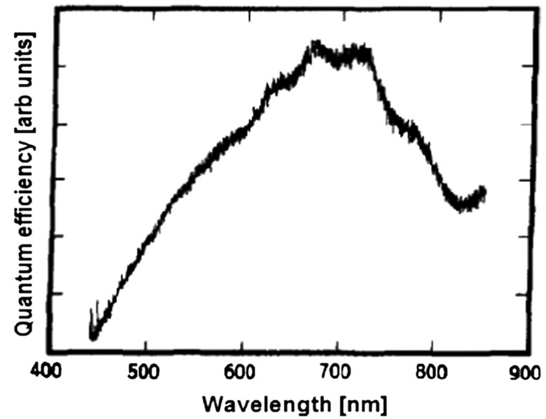

Fig. 3 Emitted spectrum as of a 5×1 micron line width CMOS integrated CMOS avalanche LED (after Kramer et al. and Snyman et al.).

1. Good dynamic range in optical signal detection
   With Si technology, small micro detectors of high sensitivity can be fabricated between 450 and 750 nm. The leakage currents of small 10×10 micrometer detectors are in the order of pico amps at room temperature and the low-frequency power detection levels are in the order of pW.[22] Power emission levels emitted from Si CMOS LEDs are in the order of 10 to 100 nW, which is three to four orders higher than the CMOS $p-n$ detectors can measure.
2. Bandwidth speeds greater than 1 Gb/s
   The modulation speeds of small InAv CMOS LEDs are high, because the device operates in reverse bias mode. The small dimensions of the device result in low parasitic capacitances and very high modulation speeds.[11] The modulation speed of the integrated Si LEDs in CMOS integrated circuits is determined by the surrounding driving and signal processing circuitry. Substantial progress has been made leading to GHz signal processing speeds. Optical source and sensor-based systems can hence be fabricated in CMOS integrated circuitry at moderate to high optical modulation frequencies.
3. Good electrical isolation
   Because of low leakage currents at room temperature, Si CMOS technology offers very high electrical isolation, immunity to interference, and high signal security.
4. System reliability
   Si diodes that utilize the avalanche concept in order to regulate and control voltages in CMOS integrated circuitry have been highly reliable.[9]

Figure 4 shows the layout of a simple n^+p well Si avalanche LED and interface that can feed light into the adjacently lying optically transparent field oxide layer. The light is emitted slightly below the apex of the SiO_2 "field oxide" region. The positioning of the light-emitting region ensures optimum coupling of light into the layer.

Special detectors have been designed to ensure optimum detection efficiency for laterally incident radiation.[15]

It follows, consequently, that much more advanced and more favorable electro-optical structures can be designed and fabricated utilizing CMOS technology.

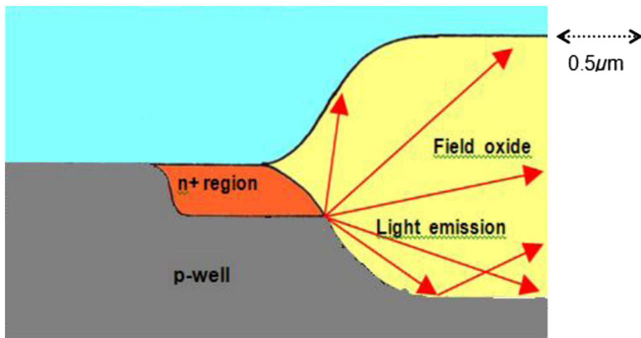

Fig. 4 Design of an initial line source Si LED positioned at the "bird's beak" in Si CMOS structure.

4 Optical Propagation and Refraction Phenomena In CMOS Integrated Circuit Structures

Since most optical simulation tools, such as those available on the free market today, are designed for application in the macro environment, we opted to design our own initial software tool for specific application in CMOS structures and dimensions. The commercial tools are also mostly designed for application in the macro-optical environments while a custom-designed tool would offer better customization and adaptation to targeted needs. This also offered additional design flexibility and better understanding of our analysis, as compared to merely utilizing available "ray tracing" software.

Our group subsequently used MATLAB[29] to geometrically develop specific CMOS structures of specific optical properties and to evaluate the optical refraction and optical propagation phenomena in such structures.

A special ray tracing program was subsequently developed, which could specifically analyze the refraction and optical propagation phenomena in CMOS integrated circuit structures and identify the geometrical positioning of the optical sources within these structures. Furthermore, we could include a series of iterative propagation and scattering paths using the Monte Carlo randomization techniques. The refractive indices that were used in the optical simulation at 750 nm were: 1.00 for air, 2.00 for Si nitride, 1.48 for Si plasma, 1.45 for Si oxide and 3.76 for the Si substrate.[10,30]

4.1 *Domain Definition*

The domain of the modeled Si CMOS structure was defined by geometrical algebraic statements generated with MATLAB in the code called "K-Dedicated Code A." Matrix geometrical algebraic statements were used to generate the graphical preliminary matrix elements look-up table for a typical CMOS structure (see Appendix A).

Subsequently, specific substructures were developed with mathematical formulas and boundaries. This approach subsequently led to:

- faster generation of the final matrix look-up table;
- more versatility with respect to the graphical user interface to quickly change the structure dimensions, composition, and refractive index; and
- an ability to generate many new structures with different geometrical designs.

The geometric blocks used to build up the structure were limited to basic triangular and rectangular shapes, because CMOS structures can be generated and modeled by these shapes effectively. As for the triangles, two sides (TSIDE_1 and TSIDE_2), one angle (TANGLE12) in between the sides, and one vertex (TVERTEX1) were the parameters used to construct the various triangles. Likewise for the rectangles one, vertex (RVERTEX1) and two sides (RSIDE1 and RSIDE2) were used to construct the various rectangular shapes involved in the generation of the CMOS structure.

Figure 5(b) subsequently illustrates how a complex new CMOS structure was eventually generated using a number of the pre-defined sub-block structures, each defined with particular dimensions, refractive index, and color information.

4.2 *Stepping Algorithm Development*

A stepping algorithm was developed as a subroutine within the "K-dedicated code B" and applied to multiple rays, each with a different initial launch angle. Snell's and Fresnel laws were applied as basic physical laws governing refraction, reflection, and even for determining polarization characteristics.[31]

For the total internal reflection of the rays within the structure, the critical angle for internal reflection was used as

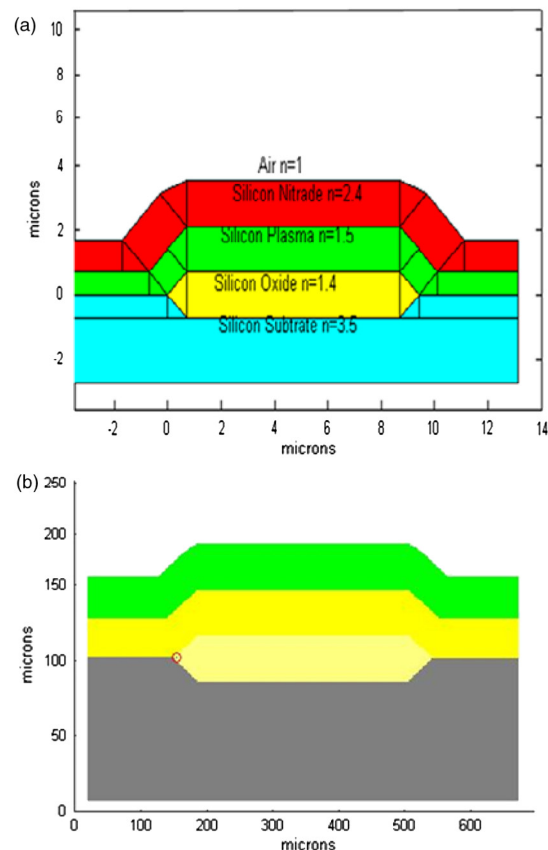

Fig. 5 (a) Developing geometrical building blocks for generating a CMOS test structure and (b) generation of a unified matrix that could be used for Monte Carlo simulation (1st layer (from top) = silicon nitride; 2nd layer = inter-metallic plasma oxide; 3rd layer = field oxide; substrate = silicon.

$$\sin \theta_c = n_2/n_1, \tag{1}$$

where θ_c = critical angle.

For detailed reflectance calculations, the following Fresnel equations were used:

$$E'/E = \frac{\cos \theta - (n^2 - \sin^2 \theta)^{1/2}}{\cos \theta + (n^2 - \sin^2 \theta)^{1/2}} \tag{2}$$

for transverse electric (TE) polarization, and

$$E'/E = \frac{-n^2 \cos \theta - (n^2 - \sin^2 \theta)^{1/2}}{N^2 \cos \theta + (n^2 - \sin^2 \theta)^{1/2}} \tag{3}$$

for transverse magnetic (TM) polarization and where θ was the launch angle from horizontal.

The concepts of Monte Carlo-based randomization[32] were subsequently also incorporated in the stepping algorithm. This algorithm progressively performs a stepping function in which a new propagation position and new launch angle is defined based on the local matrix information values. If a change of refractive index did occur, the incident angle to the interface was determined, Snell's law for refraction and Fresnel laws for reflection were applied, and new rays with new propagation positions and launch angles were defined within the larger matrix. An example of the program code for determining refraction when encountering an interface is shown in Program Snippert 2 (See appendix A).

$$x'_{x+1} = a_1 x'_1 + c_1 (\text{modulo}\, n) \tag{4}$$

Figure 6 shows some of the ray propagation analyses, which were observed when the optical source was placed at the bottom of the first Si-SiO_2 interface. A certain amount of tilt of the overlaying plasma oxide and passivation nitride was assumed. The pertinent observations were the following:

1. Clear propagation paths were portrayed for each ray. All rays propagated parallel in real time and progressive reflections and refractions could be followed.
2. The multiple-ray approach demonstrates the overall optical performance of the structure.
3. The Si nitride layer, which had the highest refractive index of all the over-layers, refracted the light beam the highest. The dispersion of the vertically emitted rays is high toward the right side of the structure in Fig. 6. This is more pronounced when shorter wavelengths are used. The shorter wavelengths experience a higher degree of dispersion. When the Si nitride layer in Fig. 6 is not tilted, the rays are emitted from the structure into the air in a quite undisturbed manner.
4. When the angle of incidence into the Si nitride layer exceeds the critical angle, total internal reflection occurs at the top of the Si nitride interface, leading to backward scattering into the Si substrate.
5. In the Si nitride layer (left-hand side of the structure in Fig. 6) the optical rays are wave-guided. The Si nitride layer is transparent for wavelengths longer than 600 nm. The transparent wavelength range in Si nitride stretches from 600 to over 1500 nm.[30] The absorption as a function of wavelength still has to be investigated.

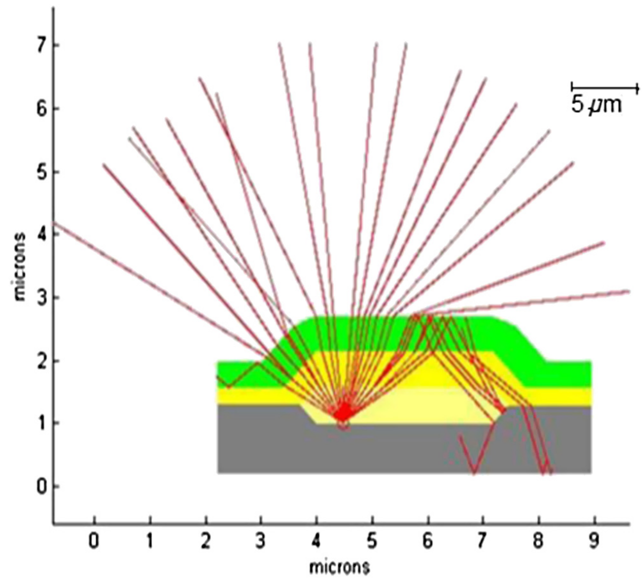

Fig. 6 First iteration of optical propagation observed in a scaled unified CMOS Si LED test structure.

Figure 7 shows the propagation of the optical rays when the optical source is shifted slightly to the left along the Si-plasma deposited oxide interface. Improved coupling was observed into the Si nitride layer. Total internal reflection is observed for some of the waves in the Si nitride layer.

Figure 8 shows the ray propagation when the thickness of some of the field oxide and plasma deposited oxide layers was increased. The optical propagation in a variety of CMOS structures was subsequently investigated. The vertical thickness of the layers was varied. Figure 8 also demonstrates that the optical power could be separated into two different paths. A certain percentage of the radiation escaped out of the design, while the rest was emitted laterally into the Si nitride layer. Optical splitters of this kind have diverse applications

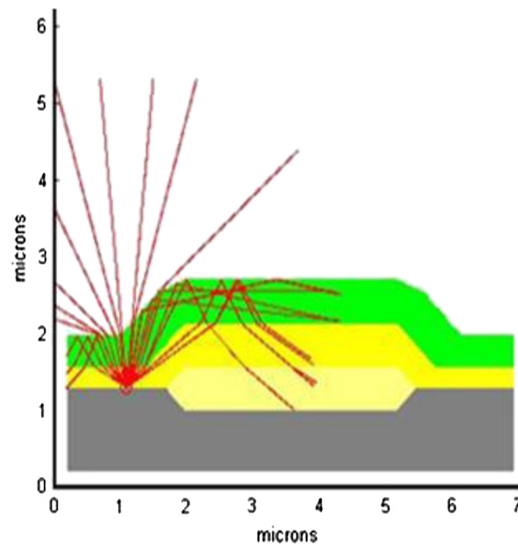

Fig. 7 Effect of changing of optical emission point source in a Si LED CMOS structure.

in MOEMS and can be used for interference and phase contrast.

Figure 9 shows a structure in which the curvature caused by the field oxide layer was utilized. The optical source is positioned in the middle of the hemispherical structure. The launch angles for the rays range from 30 deg[t] to 150 deg. The radiation is emitted under a solid angle of 120 deg.

The estimated optical emission factor of the Si-SiO_2 interface source is approximately 0.40. Minor scattering is observed due to surface bending irregularities at the Si nitride-air interface and absorption losses occur in the Si nitride layer at shorter wavelengths.

Figure 10 shows a similar structure, but here the light source emitter position is shifted. When the source is placed at position A, near to the "bird's beak" field oxide layer, the rays emitted vertically from the structure are slightly focused. When the source is placed at position B, the radiation is emitted toward a 45-deg slanted angle.

Figure 11 demonstrates optimized wave-guiding of the total emitted Si LED radiation inside the Si nitride layer. The plasma deposited oxide layer thickness has been reduced and the optical emission point was positioned near the "bird's beak" point in the Si oxide layer. Ray launch angles ranging from 34 deg to 76 deg couple effectively the optical radiation into the Si nitride layer. Because of the lower refractive indices of both the plasma-deposited and field-oxide layers below and above, the optical rays can effectively propagate inside the Si nitride layer. Si nitride is transparent for wavelengths above 600 nm. Si oxi-nitride (SiO_xN_x is also transparent at lower wavelengths.[25,30] In both cases, the wavelength of the wave-guided radiation is much lower than the absorption edge wavelength for Si detectors (1100 nm). The combination of an Si LED light source, an optical waveguide, and an Si detector can hence be incorporated with ease into the same structure. A particular CMOS microphotonic structure can hence be realized in the CMOS integrated circuitry.

The current total optical emission levels from our Si CMOS LEDs are in the order of 1 to 100 nW. These power emission levels are much higher than the low power detection level of Si $p - n$ detectors.

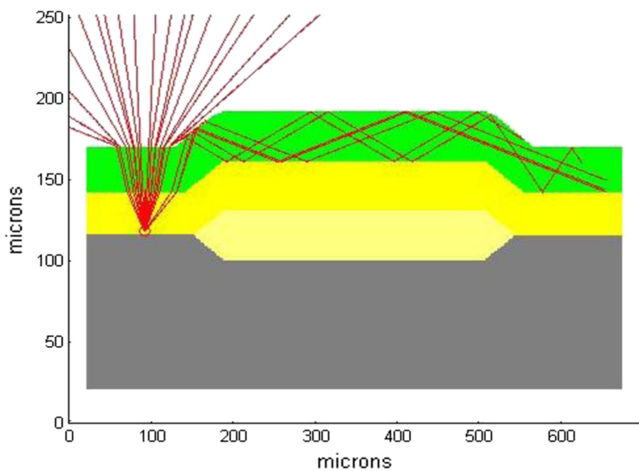

Fig. 8 Change of layer thickness and its effect on the propagation in an Si LED CMOS structure.

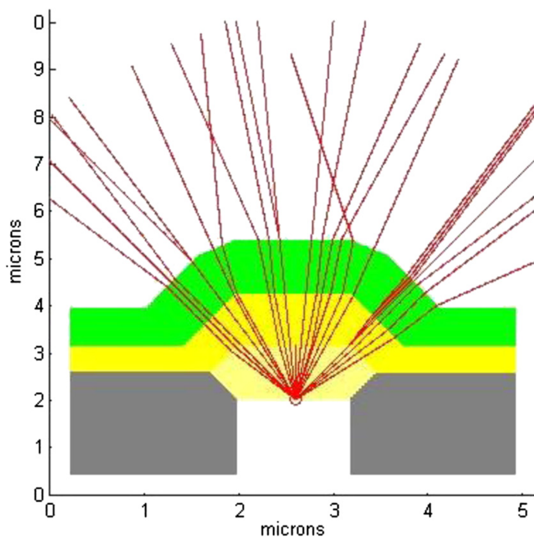

Fig. 9 Maximizing vertical optical emission from a CMOS Si LED structure.

5 Designing Lateral Waveguides for CMOS Structures

CMOS technology below 0.35 μm can also be utilized to design lateral waveguides. CMOS designs below 350 nm are planarized after the MOSFET transistor fabrication. Up to

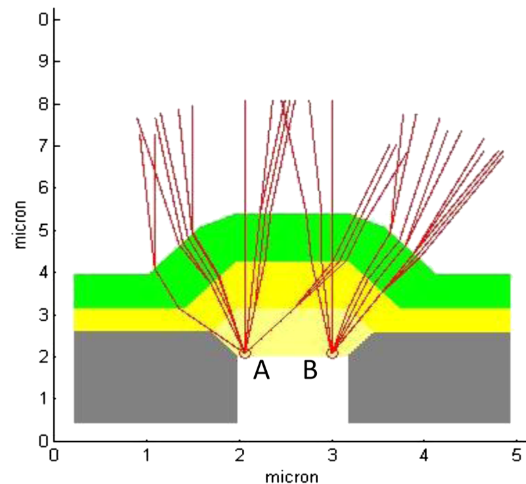

Fig. 10 Directional focusing from predetermined sources.

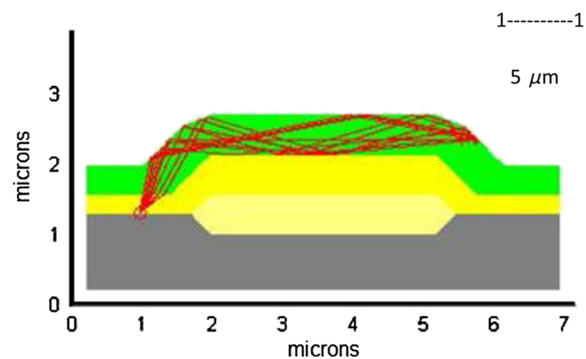

Fig. 11 The effect of the layer thickness on the propagation in a Si LED CMOS structure.

six metal layers are deposited on top of these layers, where sloping of the outer layers is caused by the thicker outer metal layers.[23] This technology uses trench isolation for electrically isolating *n*- and *p* MOSFETS laterally in the CMOS structure. The trench-isolation technology opens up interesting optical properties. Trenches are spatially defined by RF etching followed by oxide lining and subsequent plasma deposition of Si oxides. If these trenches could be filled with an optical material of higher refractive index, optical radiation emitted from the Si-overlayer interface, could then be coupled with high efficiency directly into the adjacent optical channels. The current CMOS technology can create a thin oxidation layer that is used as an isolation layer in the trench technology. If this layer is enhanced and followed by a layer of high refractive index material, such as Si nitride, interesting lateral optical conductors and waveguides can be constructed at the Si–overlayer interface. Optical sources positioned at the edges of the trenches enable optimum coupling of optical radiation into the trench waveguide. In a similar way waveguides can be fabricated in the outer CMOS layers. Figure 12 schematically illustrates these concepts.

We used advanced optical simulation software (RSOFT Beam PROP)[34] to design and simulate specific CMOS-based waveguides operating at 750 nm based on CMOS materials and parameters. This software uses an advanced finite analysis method where the volume is divided up into a large number of matrix elements. Helmholtz's equation predicts the optical parameters along the matrix based on the initially defined optical fields.

We performed a number of optical simulations in CMOS structures with 0.2 to 0.6 μm-wide channels, embedded in 1.5-μm diameter Si oxide. The operating wavelength was 750 nm. A flat emission surface with wide-angle emission were used at the edge structure of the Si nitride, in order

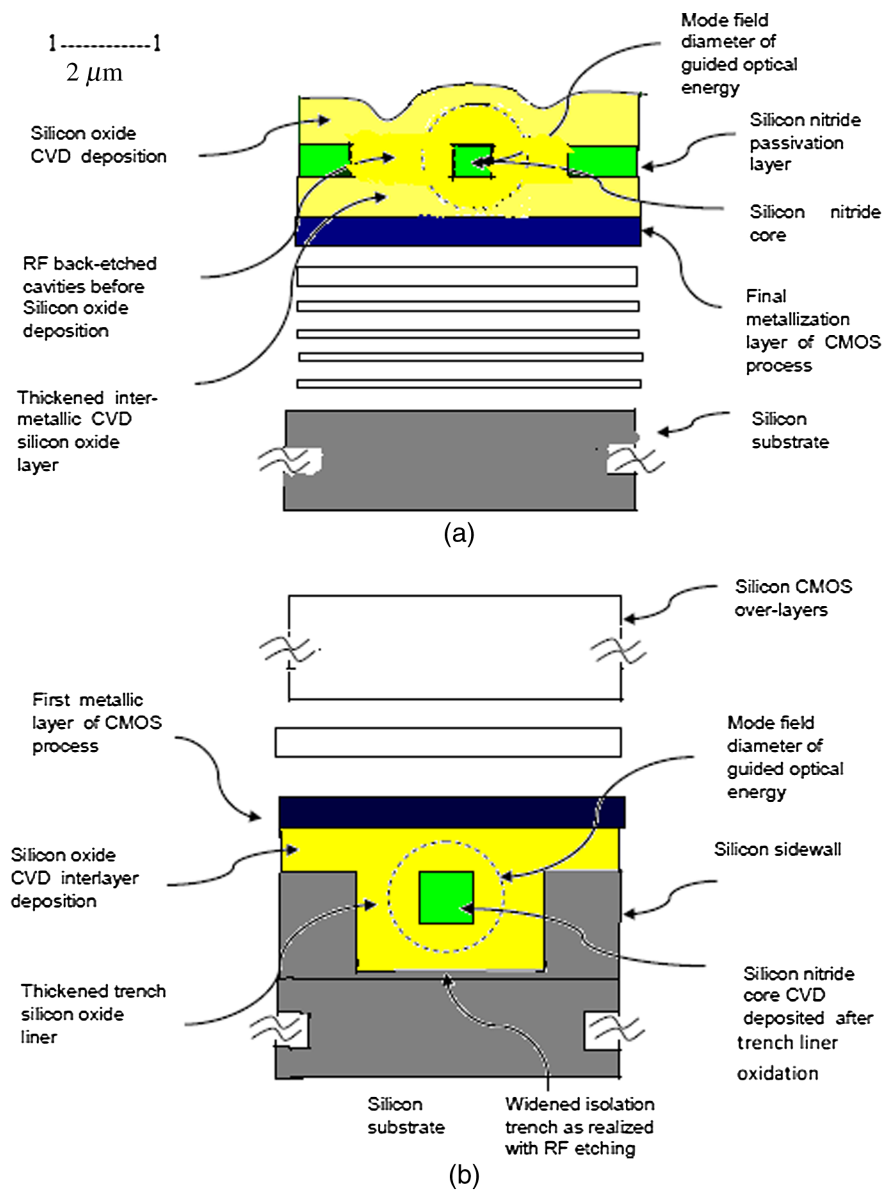

Fig. 12 Cross-sectional profiles of waveguides that can be constructed with existing CMOS processes. (a) Waveguide structure fabricated by post processing and/or B-pad processing of the over layers. (b) Trench-based waveguides with Si nitride embedded in Si oxide. (see Ref. 33)

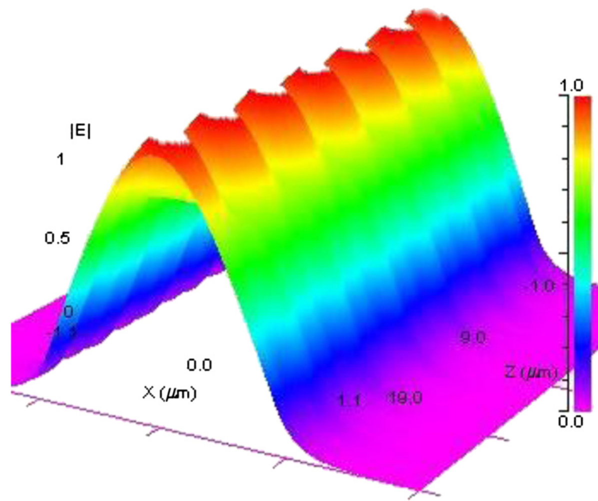

Fig. 13 Advanced optical simulation of the electrical field propagation in a 0.5-μm-wide Si nitride layer embedded in SiO_2 in CMOS integrated circuitry using finite element analysis and solutions of Helmholtz's equation. Multi-mode optical propagation at 750 nm is demonstrated over 20 μm distance with a loss smaller than 1 dB $\cdot$ cm^{-1}.

to simulate the emission characteristics of our Si avalanche LED source best.

Our preliminary results show that multimode, as well as single mode wave-guiding can be achieved. Figure 13 shows a three dimensional view of the electrical field along the waveguide of a 0.6 μm wide Si nitride waveguide. Multimode propagation is demonstrated with almost zero loss up to a distance of 20 μm. Multimode propagation in CMOS micro systems has the advantage of having a large acceptance angle for coupling optical radiation from a Si LED into and out of a waveguide. Our calculations show that a coupling efficiency of 0.38 can be achieved for a flat Si-emitting surface positioned at the edge of the Si nitride core of the waveguide. This is mainly due to the better refractive index matching between Si (3.76 at 750 nm wavelength) to Si nitride (2.00 at 750 nm).

Figure 14 shows the predicted optical simulation for a 0.3-μm diameter Si oxi-nitride waveguide embedded in Si oxide. The two-dimensional plot of the electrical field propagation along the waveguide shows clearly single-mode propagation. The calculated loss curve in the adjacent figure shows almost zero loss over a distance of up to 20 μm. The coupling efficiency into such a waveguide is, however, much reduced to values of about 0.05. Multimode to single-mode converter structures can, however, be used to increase overall coupling efficiency into the waveguide.

Figure 15 displays the mode field pattern in the waveguide perpendicular to the axis of propagation. With the values derived from the simulations for the real part of the propagation constant, an accurate energy loss could be calculated with conventional optical propagation physics. Low loss of 0.65 dB $\cdot$ cm^{-1} is predicted at 650 nm. At shorter wavelengths from 450 to 650 nm much higher losses of more than 1 dB $\cdot$ cm^{-1} are predicted because of the higher absorption coefficient in Si nitride at these wavelengths. The bandwidth-length product could be derived from the calculated effective refractive index and predicted modal dispersion values calculated by RSoft BeamProp (Fig. 14). The calculations predict a bandwidth-length product of approximately 200 GHz-cm.

With a short wavelength and high refractive index difference between core and cladding (1 μm in diameter), a high level of micro bending can be achieved. Since with CMOS technology many different over-layers can be deposited on top of each other, optical energy can easily be coupled between waveguides and optical sources near the Si over-layer interface to layers higher up in the structure.

Another feature that was investigated was the positioning of a two-dimensional Si nitride lens at the end of the waveguides. Such a design can be used to obtain two- and three-dimensional control of the optical radiation at distances of up to 10 μm away from the end of the waveguide. Figure 16 demonstrates "focusing" of the optical radiation from a single-mode Si nitride waveguide.

These initial simulations of Si nitride waveguides in CMOS technology are extremely promising. All the latter

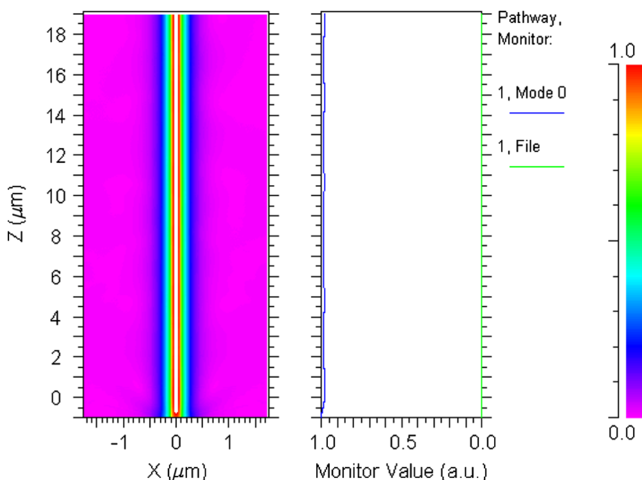

Fig. 14 Simulation of the optical field propagation in a Si nitride layer in CMOS integrated circuitry using finite element analysis and solutions of Helmholtz's equation. Single-mode optical propagation is demonstrated at 750 nm over a distance of 20 micron for a 0.2-μm wide, Si-oxide-embedded and Si nitride waveguide.

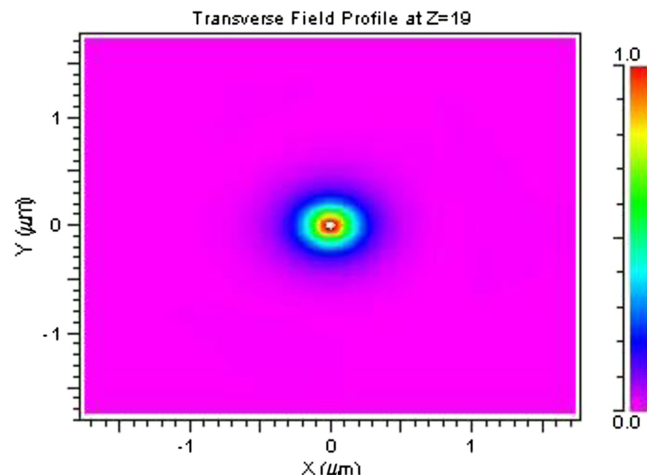

Fig. 15 Mode field diameter predictions for a Si nitride CMOS-based waveguide with a core of 0.2 μm diameter embedded in a 1 μm diameter Si oxide cladding.

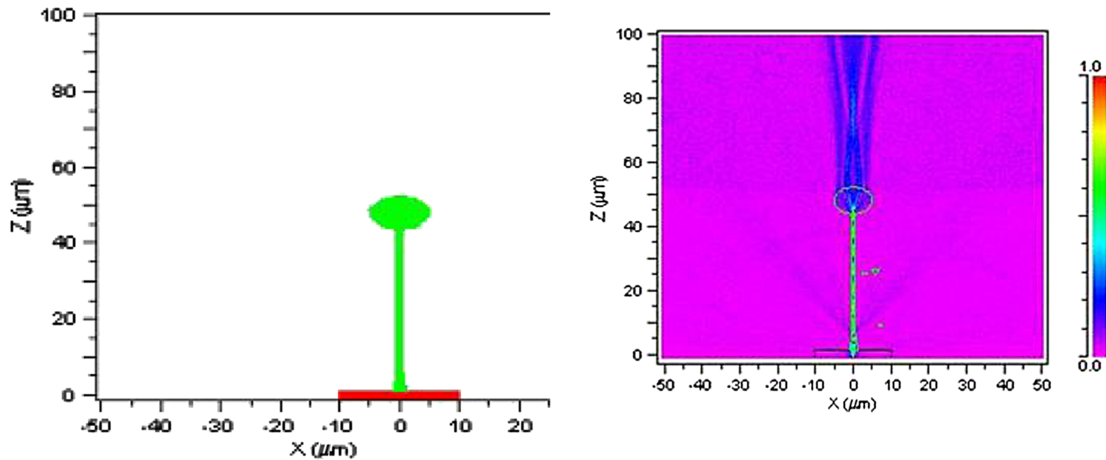

Fig. 16 Far field manipulation of the optical radiation passing through a two-dimensional Si nitride lens placed at the end of a CMOS waveguide.

designs can be applied to CMOS-based microphotonic systems.

6 First Iteration Experimental Results

Figure 17(a) and 17(b) display an optical emission micrograph as observed vertically upward into the microscope objective and as emitted from a 0.35 μm CMOS structure as shown in Fig. 17(b). This CMOS structure closely resembled the cross-section over-layer structure presented in Fig. 18. The emission occurred at a n^+p junction interface adjacently to the field oxide layers. Interesting features as observed are the following:

A very bright vertical emission was observed. This emission is a result of the vertical emission characteristics as simulated in Fig. 7. The total optical emission power of 100 nW was observed for these structures using a calibrated Si $p-i-n$ detector. Red light was observed at one side next to the vertical emission. This indicates that more red light were refracted into the acceptance angle of the microscope, while the blue light was refracted toward the surface of the structure. This correlates with the simulation results as obtained in Fig. 6, which demonstrated less dispersion of emitted light vertically outward from CMOS structures with a silcon nitride top layer and high dispersion along the surface of the chip for shorter wavelengths. This observation, therefore, indicates good correlations between the optical simulation results as predicted by our optical simulation techniques.

Figure 18(a) and 18(b), demonstrates a first iteration optical link as was realized in Si 1.2-μm CMOS integrated technology over a distance of 150 μm. The optical source was of the type as demonstrated in Figs. 2 and 4. The CMOS waveguide design was similar to the one presented in Figs. 11 and 12(a). Optical coupling was realized into the top Si nitride layer similar to what was demonstrated in Fig. 8. The detector was a custom-designed Si detector, of 10×10 μm dimension, and optimized for lateral incidence.

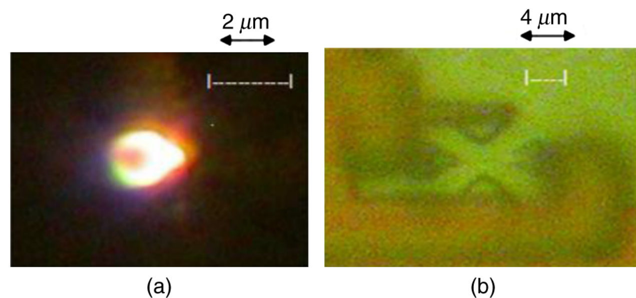

Fig. 17 (a) and (b) Photomicrograph of optical emissions observed from top of an injection-avalanche Si CMOS LED.

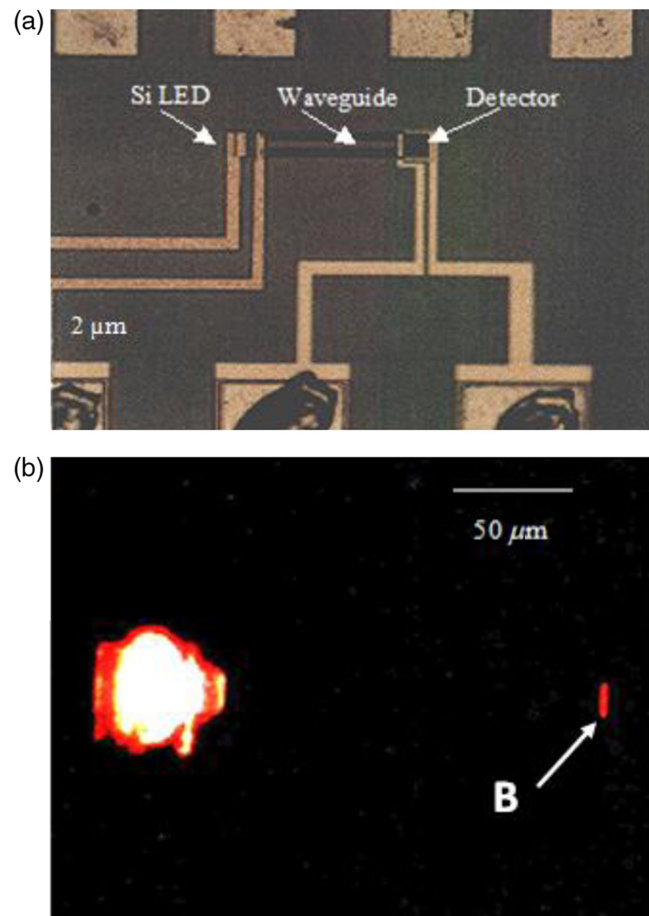

Fig. 18 Photomicrographs of a CMOS opto-coupler arrangement consisting of a CMOS av-based light-emitting source, an optical waveguide and a CMOS lateral incident photo detector. (a) Shows a field photo-micrograph of the arrangement, and (b) shows the optical emission output as observed under dark field conditions.

Some first iteration results with regard to this realization have been published elsewhere already.[21]

This particular realization was achieved in the Carl and Emily Funch Institute of Microelectronic Laboratories University of Pretoria in South Africa. We have recently achieved similar results in ESIEE Labs in France (Europe). This is currently the topic of further research.

When the Si LEDs were pulsed at low frequencies (below 1 kHz), signal levels were ranging from 6 nA to 100 nA. When phototransistor detectors were used, signal levels were detected of about 1 μA. No signals were observed at the detector when the voltage pulses were repeated at these voltage levels, but without optical emission. It should be appreciated that these results are first iterations. The photomicrograph shows high losses at the optical source. Assuming a detector efficiency of 0.3 W/A, and coupling efficiencies of 0.1 from the source to the waveguide, as well as a loss of 0.75 $\text{dB} \cdot \text{cm}^{-1}$ at 750 nm for wave guiding in the Si nitride layer itself, indicate source optical power in the 100 nW range. This correlates with our earlier optical measurements for vertical emission from our Si Av LEDs as in Fig. 17. The loss characteristics for the waveguide correlate with loss characteristics for Si nitride at 750 nm as determined by Gorin et al.[30] These analyses provide an important basis for further developments.

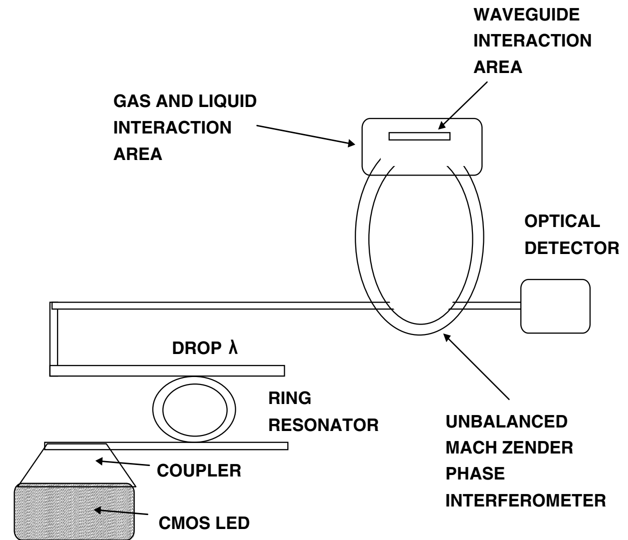

Fig. 19 Schematic diagram of a CMOS-based microphotonic system that can be realized using an on-chip Si Av LED, a series of waveguides, ring resonators, and an unbalanced Mach-Zehnder interferometer. A section of the waveguide is exposed to the environment and can detect phase and intensity contrast due to absorption of molecules and gases in the evanescent field of the waveguide (see Refs. 35, 36).

7 Applications of Si Av LEDs and CMOS Waveguides at 750 nm in CMOS-Based Microphotonic Systems

It follows that the described technologies can be integrated either in hybrid or monolithic form in standard CMOS designs, realizing various microphotonic systems and/or MOEMS. Si LEDs and associated electronic processing circuitry can be integrated into standard CMOS technology allowing mass production at low cost. Optical modules and CMOS technology can be integrated in hybrid form using RF recess technology. With waveguide technology, whole MOEMS structures can be grown monolithically on CMOS circuits. MOEMS ranging from vibration sensors, motion and accelerometer sensors to more advanced chemical, physical, and biosensor as well as nanotechnology devices can be constructed. These applications are illustrative at this stage, but nevertheless demonstrate some interesting possibilities and applications.

In Fig. 19 a hypothetical microphotonic system is demonstrated that consists of an Si LED, a Si detector together with waveguides integrated monolithically in a CMOS structure.[35] Wide area Si LEDs are used in order to increase the total optical emission power into the waveguide systems. Appropriate filtering by means of ring resonators, and enhanced phase contrast detection can be obtained by utilizing unbalanced Mach-Zehnder interferometers. Near the end of the layout, an opening is integrated in the CMOS overlayers by post processed RF etching, that enables gas or liquids to interact with the evanescent field of a waveguide section and introduces intensity and/or phase contrast changes. Adjacent digital and analog circuitry processes the observed information. Hence, a complete microphotonic sensor system can be integrated into standard CMOS circuitry. The added intelligence component, the lowering in cost and the increase in reliability of such systems can be significant.

Figure 20 demonstrates a more explicit and hypothetical MOEMS system. The system consists of a Si CMOS LED, an array of Si detectors and a series of CMOS-based waveguides. A mechanical arm is RF etched into the structure by postprocessing. Radiation is directed at an angle onto the mechanical arm, and the reflected light is sensed by an array of CMOS detectors. Such a system can detect vibration, acceleration, and axial rotation and relate these to electronic output signals.

Similarly, in the cavity optical absorption measurements, fluid flow and gas flow as well as fluorescence experiments of samples can be performed by arranging source and detector and waveguide arrays on the side surfaces of

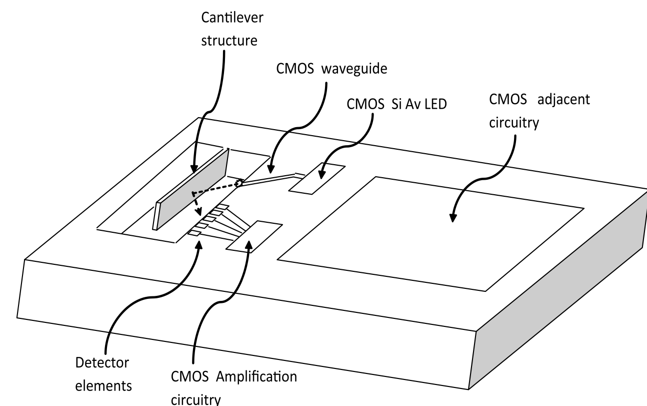

Fig. 20 Schematic diagram of a CMOS-based MOEMS that can be realized with conventional CMOS integrated design and additional post processing. Key constituents of such a device are an effective CMOS on-chip optical source, coupling of the source to a waveguide, CMOS compatible optical wave guiding and optical collimation and detection circuitry (see Refs. 36, 37).

the cavity. The potential applications are diverse and can be linked to emerging fields, such as bio- and nanotechnology.

8 Conclusions

1. MATLAB and BEAMPROP based software simulation tools were utilized for the evaluation of optical propagation and refraction phenomena in complementary metal oxide semiconductors (CMOS) Si structures, for 1.2-μm, 0.35-μm and below 0.35-μm technology. For 1.2- and 0.35-μm technology, the structures incorporated extensive contouring of the outer layers that offer various design possibilities. Av Si LEDs, which emit between 450 to 850 nm were used as light sources in the analysis and the characteristics of these light sources were incorporated in the analysis. Refractive indices, layer thicknesses, and layer curvatures were the ray propagation parameters.
2. A Monte Carlo method was incorporated continuously updating refraction and reflection as the optical ray propagates through the structure. The simulations showed that the vertical emission could be increased from a factor of 0.02 to 0.4. Further, it improved the splitting of optical radiation from a single path into two propagation paths and the wave guiding of light inside the Si nitride passivation layers. Favorable predictions were obtained with multimode as well as single-mode optical propagation at very low loss of below 0.75 $\text{dB} \cdot \text{cm}^{-1}$ and very low modal dispersion, enabling bandwidth length products of up to 100 $\text{GHz} \cdot \text{cm}$.
3. Favorable correlations were obtained between simulation predictions and experimental observed results for the vertical optical emissions from Si LEDs and waveguides.
4. A CMOS-based optical link was demonstrated utilizing an avalanche-based Si LED, and a specially designed CMOS-based waveguide and CMOS-based detector for the 600 to 850 nm range. On-chip optical coupling was verified by experimental analyses.
5. The potential applications of 600 to 850 nm Si LEDs and 600 to 850 nm-based waveguides in custom-designed CMOS-based microphotonic systems and MOEMS were demonstrated. The competitive advantage offered by this technology, is that all components, including the optical source, the optical paths, the mechanical module as well as the detectors can be fabricated on the same chip at micro-dimension level into standard silicon CMOS integrated circuitry.

Appendix A

PROGRAM SNIPPERT 1 //Pseudo-code/block of flow diagram for domain definition//

```
max X = 160;
size X = max X * 10;
max Y = 116.4; %Fixed
size Y = max Y * 10;
x = 0:size X;
y = 171 - 50 + (x - 50) * (x > 50) - (x - 100)*
(x > 100);
z = 134 - 50 + (x - 50) * (x > 50) - (x - 100)*
(x > 100);
q = 98 - 50 + (x - 50) * (x > 50) - (x - 100)*
(x > 100);
s = 53 - 50 + (x - 50) * (x > 50) - (x - 100)*
(x > 100);
yn = -y;
zn = -z;
qn = -q;
sn = -s;

refractiveindices = [1   2.4   1.5   1.4   3.5   3.5   3.5];
for j = 1: size X%Column
  m = 1;
    for k = (-201 + 0.345:0.345:201 - 0.345)
      if k > y(j)
        Body1(j, m) = refractiveindices(1);
      else if(k > z(j)) & &(k < y(j))
        Body1(j, m) = refractiveindices(2);
      else if(k < q(j)) & &(k < z(j))
        Body1(j, m) = refractiveindices(3);
      else if(k < s(j)) & &(k < q(j))
        Body1(j, m) = refractiveindices(4);
      else if(k < sn(j)) & &(k < qn(j))
        Body1(j, m) = refractiveindices(6);
      else if(k < qn(j)) & &(k < zn(j))
```

PROGRAM SNIPPERT 2 //Pseudo code or flow diagram for structure shape generation//

```
RT = 1;
figure(1)
axis equal
INCLINATIONCHECK = 45; %67.5;
ANGLECHECK = 90; %45;
ANGLECHECKHALF = 45; %22.5;
VERTEXMATRIXX = □eros(4, 1);
VERTEXMATRIXY = □eros(4, 1);
BLOCKSHAPE = [];
BLOCKNUMBER = 1;

BLOCKSHAPE(BLOCKNUMBER) = 0; %0 for triangle
TVERTEX1 = [0; 0];
TSIDE1 = RT;
TSIDE2 = RT;
TANGLE12 = ANGLECHECK;
TROTATION = INCLINATIONCHECK;
TCOLOR = 'y';
REFRACTIVEINDEX(BLOCKNUMBER) = 1.4;
[a   b] = trblock(TVERTEX1, TSIDE1, TSIDE2,
TANGLE12, TROTATION, TCOLOR,
REFRACTIVEINDEX);
VERTEXMATRIXX(:, BLOCKNUMBER) = [a; 0];
VERTEXMATRIXY(:, BLOCKNUMBER) = [b; 0];
fill(a, b, TCOLOR)
hold on
BLOCKNUMBER = BLOCKNUMBER + 1;

BLOCKSHAPE(BLOCKNUMBER) = 1; %1 for rectangle
[xs, ys] = getstart(a, b, 2);
RVERTEX1 = [xs; ys];
RSIDE1 = RT * 3;
```

```
    RSIDE2 = RT * cos d(INCLINATIONCHECK) * 2;
    RROTATION = 90;
    RCOLOR = 'y';
    PROGRAM SNIPPERT 3 //Fresnel formula for refraction
and Snell's law of reflection//
    bb = anglenextpoint(f);
    if abs(BODY2(yy(step, f), xx(step, f))/BODY2
(yy(step + 1, f), xx(step + 1, f))*
sin d(90 + inc(f) − anglenextpoint(f))) <= 1
        anglenextpoint(f) = 90 + inc(f)−a
 sin d(BODY2(yy(step, f), xx(step, f))/BODY2(yy(step +
1, f), xx(step + 1, f)) * sin d
(90 + inc(f) − anglenextpoint(f)));
        sign R = 1;
        FLAG = 0;
    else
    disp('REFLECTION')
    if anglenextpoint(f)−
inc(f) > 90 & anglenextpoint(f) > 90

      anglenextpoint(f) = −anglenextpoint(f) + 2 * inc(f);
    elseif

anglenextpoint(f) − inc(f) < 90 & anglenextpoint(f) > 90

      anglenextpoint(f) = anglenextpoint(f) − 2 * inc(f);
    elseif

anglenextpoint(f) − inc(f) > 90 & anglenextpoint(f) < 90
      anglenextpoint(f) = anglenextpoint(f) − 2 * inc(f);
    elseif

anglenextpoint(f) − inc(f) < 90 & anglenextpoint(f) < 90

      anglenextpoint(f) = −anglenextpoint(f) + 2 * inc(f);
          end anglenextpoint(f)
    xx(step + 1, f) = xx(step, f);
yy(step + 1, f) = yy(step, f);
      a(f) = BODY2(yy(step, f), xx(step, f));
        FLAG = 1;
    En
```

Acknowledgments

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Kingsley A. Ogudo received the NDip, NHD, BTech degree and MTech degree, all in electrical and electronics engineering from Federal Polytechnic, Nigeria and the Tshwane University of Technology (TUT), South Africa, in 1998 to 2010. During the period 2003 to 2005 he was with the French South African Technical Institute in Electronics (F'SATIE) completing his BTech courses and studying in opto-electronics and telecommunications technology. Since 2008, he is a graduate lecturing assistant as well as research assistant at the Department of Electrical Engineering at Tshwane University of Technology (TUT), South Africa. His research interest includes electronic, optoelectronic devices, telecommunication engineering high-frequency electronics, physics, and mathematics. He is currently registered for his DTech studies on "Simulation of Si LED's (450 nm to 750 nm) Light propagation phenomena in CMOS 0.35 micron integrated circuitry-MOEMS applications" under the supervision of Professors Snyman, Prof. T. Bourouina, Dr. D. Schmieder and Prof. D. Foty.

Diethelm Schmieder obtained his Dipl-Phys. (MSc in physics) in 1974 from the Christian-Albrechts University Kiel, Germany, and his PhD (physics) in 1991 from the University of Natal Pietermaritzburg, South Africa. His research interests are lasers, high power fiber lasers, short pulse fibre lasers, fibre Bragg gratings, photonic crystal fibres, super-continuum, and waveguide beam propagation. At the Photonics Research Group, University of Johannesburg, South Africa, he was involved in research and development of erbium doped fiber lasers, active and passive mode-locking of erbium doped fiber lasers, short pulse fiber lasers, figure-of-eight lasers, photonic crystal fibers, applications of photonic crystal fibers in mode-locking and generation of a supercontinuum, investigating fiber optical gyroscopes(FOG). At the moment he is lecturing at the Tshwane University of Technology, and involved in research concerning optical beam propagation in waveguides as fabricated on CMOS chips.

Daniel Foty is the president of Gilgamesh Associates, LLC, a technology consulting and research firm, and the chief technical officer (CTO) of a new start-up company, Sarissa Radio, Inc., which is developing new technologies for ubiquitous ultra-high-speed, low-power, low-cost wireless interconnectivity. He is the author of the best-selling book, MOSFET Modeling with SPICE: Principles and Practice, which was published in 1997 by Prentice-Hall and is now in its third printing; a Vietnamese language edition was published in early 2006. In addition, he has authored or co-authored some 100 journal articles and conference presentations, and is a frequent plenary/keynote speaker at major international conferences throughout the world. He holds the BS degrees in physics and chemistry from Bates College, the MS degree in electrical engineering from the University of Illinois, and the PhD degree in materials science from the University of Vermont.

Lukas W. Snyman received the BSc, BSc Hons., MSc and PhD degrees, all in semiconductor physics, from the University of Port Elizabeth, South Africa. During the period 1990 to 2000. Since October of 2000, he is professor at the Tshwane Technical University of Technology (TUT) in South Africa. His research interest includes opto-electronic devices, CMOS IC design, and micro-wave and high-frequency electronics. He has to date published about 80 scientific articles, mostly in international conference proceedings and scientific journals. He is also author of a chapter "Silicon CMOS Micro-photonic Systems" in a book Optoelectronics and Applications as published by Intech during 2012. He is the main author of two granted U.S. A Patents, six USA Patent Applications , and author and co-author of about ten South Africa Patents on the topic of CMOS light emitting devices. He was the main supervisor for the research as conducted in this research project.