1X Deep UV Lithography With Chemical Amplification for 1-Micron DRAM Production

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ABSTRACT

This paper describes methods used and results obtained in the production of 1-megabit (Mb) DRAM chips, using a chemically amplified tertiary-butoxy carbonyl hydroxystyrene (t-BOC) resist and 1X lithography. The internally developed resist provided high sensitivity and contrast, for 1 μm resolution on a Perkin Elmer Micralign model 500 (PE 500) in the deep UV. Characterization, and modification of the PE 500 were required for this first application in the deep UV. The manufacturing process had photo limited yield in excess of 95% with a throughput of 100 wafers per hour.

INTRODUCTION

In the early 1980s, a project to design a high performance 1-Mb DRAM was undertaken. Piloting and early production of the design was accomplished using step-and-repeat lithographic systems. The strategy for manufacturing was to use 1X lithography on as many levels of the product to take advantage of the high throughput and existing knowledge base 1X systems offer.

High-quality fused silica 1X masks were required for this task. Deep UV pellicle materials were obtained , life-tested and manufacturing qualified.

THE RESIST

A negative-tone chemically amplified resist was used for this application. The photosensitive compound was triphenylsulfonium hexafluoroantimonate ($\phi_3S - SbF_6$). The resin was a tertiary-butyl carbonate derivative of polyhydroxy styrene. This resist type requires a post-exposure bake process for image formation to occur. Sensitivity values depend on the bake conditions; i.e. higher bake temperatures and longer bake times provide higher sensitivity. The variation of image dimension with bake temperature is shown in Fig. 1, the effect of bake time on linewidth in Fig. 2, and the variation of image dimension with expose in Fig. 3.

The mechanism of image formation is illustrated in Fig. 4. Upon exposure, the triphenylsulfonium salt is decomposed to generate a strong acid. The acid reacts with

the resin to cleave the tertiary- butyl carbonate group during post-exposure bake. The images are developed with an anisole solvent rinse selectively dissolving the unexposed areas. Line width was not significantly altered by changes in the develop time. Resist adhesion was not altered by priming with hexamethyldisalizane (HMDS) or other silylating agents. In order to achieve acceptable adhesion, an oxynitride surface pretreatment was required on silicon nitride films.

The basic chemistry of this resist was described in 1982 by Ito, Frechet, and Willson at various international symposia[1,2,3].
Since that time, this chemically amplified resist scheme has been discussed in numerous publications ranging from introductory microlithography text books[4] to a current review of deep UV resist technology[5].

THE PROCESS

The process called for defining a 1 μm image in a 1.6 μm thick film of resist. After etch, a minimum of 0.7 μm resist was necessary to block the field ion implant.

Experiments were conducted to define the proper post-expose bake (PEB) temperature and time needed for line width control. Resist sidewall angle was most affected by bake temperature, with undercut profiles at low temperatures (70 °C), a 90 °C PEB was chosen to provide straight (90 °) profiles, along with a 90 second PEB time for image size control across the wafer.

Adhesion of the resist was excellent to most substrates, without the use of an adhesion promoter. A film stack of silicon nitride (Si_3N_4) exhibited marginal adhesion performance. This difficulty was avoided by converting the surface to an oxynitride layer.

In this process the PEB was the critical item for image size control and was considered the "image develop" step. Following the PEB the unexposed resist was removed using an anisole spray in a batch processing tool. This process was not critical from an image size standpoint as solubility ratio of exposed to non- exposed resist was very high. The problems encountered here had to do with defects caused by lifting resist, which would sometimes deposit back on other wafers, then causing defects.

The wafers were processed in an AME 8100 etcher using CHF_3 chemistry to define the pattern, then field ion implanted. After ion implantation the resist was stripped in an O_2 plasma.

The first-level isolation mask was a 1.0 μm design. The semirecessed oxide (SROX) isolation was defined at this level (Fig 5), the process called for an RIE etch of 1000Å Si_3N_4 to a thin pad oxide layer followed by a field implant. A 90° sidewall profile (Fig.6) was necessary to maintain the implant profile.

THE EQUIPMENT

A PE 500 with an IBM-designed interference filter for use in the deep UV was used to expose the wafers. Two of the three machines were coupled to a PEB station with a robotic handler. One of the exposure tools had a modified GCA Corp. Wafertrac bake which was manually fed.

There was not much information on the use of the PE 500 in the deep UV, as all of our experience had been in the near- and mid-UV. As we characterized the resist we also learned what modifications were needed to improve tool performance in the deep

UV. A new exposure and uniformity detector with greater sensitivity was installed to provide better dose control in the deep UV. A narrow band-pass filter was designed to provide the optimum match between the output of the capillary lamp and the resist spectral sensitivity. A new level of operating software was written to support a technique that stepped a wafer through focus, providing multiple exposures to determine optimum focus. The technique involved printing 1.0 μm contact holes while offsetting each step in focus by 10 μm in the horizontal direction. This was exposed on the entire wafer at once, allowing the reader to determine the best plane of focus. Strong shell adjustments were necessary to correct astigmatism in the deep UV. To automate and control the time from exposure to PEB, a through track coupled the PE 500 to the PEB tool. That tool had a robotic arm that took the wafer from the output track of the exposure tool and placed it on the hot plate for PEB.

The manufacturing operator could run two tools at once, loading unexposed wafers on the input elevator of the PE 500, and unloading exposed and baked wafers from the output of the PEB tool.

RESULTS

The exposure throughput achieved was 100 wafers per hour. Process-control wafers were pulled and measured while the product continued to be exposed. Exposure remained relatively constant with fluctuations primarily influenced by measurement noise and the training of new manufacturing operators. Rework was reduced to 1.5% as the process matured. Overall photo limited yield exceeded 95%. In addition, at wafer final test all electrical parametric measurements were unaffected by the the resist and its antimony based sensitizer. This last item had been the major concern in implementing this resist process.

CONCLUSIONS

A 1X deep UV lithographic process for the fabrication of 1 Mb DRAMs was successfully implemented. It extended the lifetime of existing full- field scanning systems to the manufacturing of 1 μm geometries. The experience set the foundation for future deep UV lithography.

ACKNOWLEDGMENTS

The authors thank the large number of people at IBM Almaden Research, IBM East Fishkill and IBM Burlington for their commitment to the success of this project.

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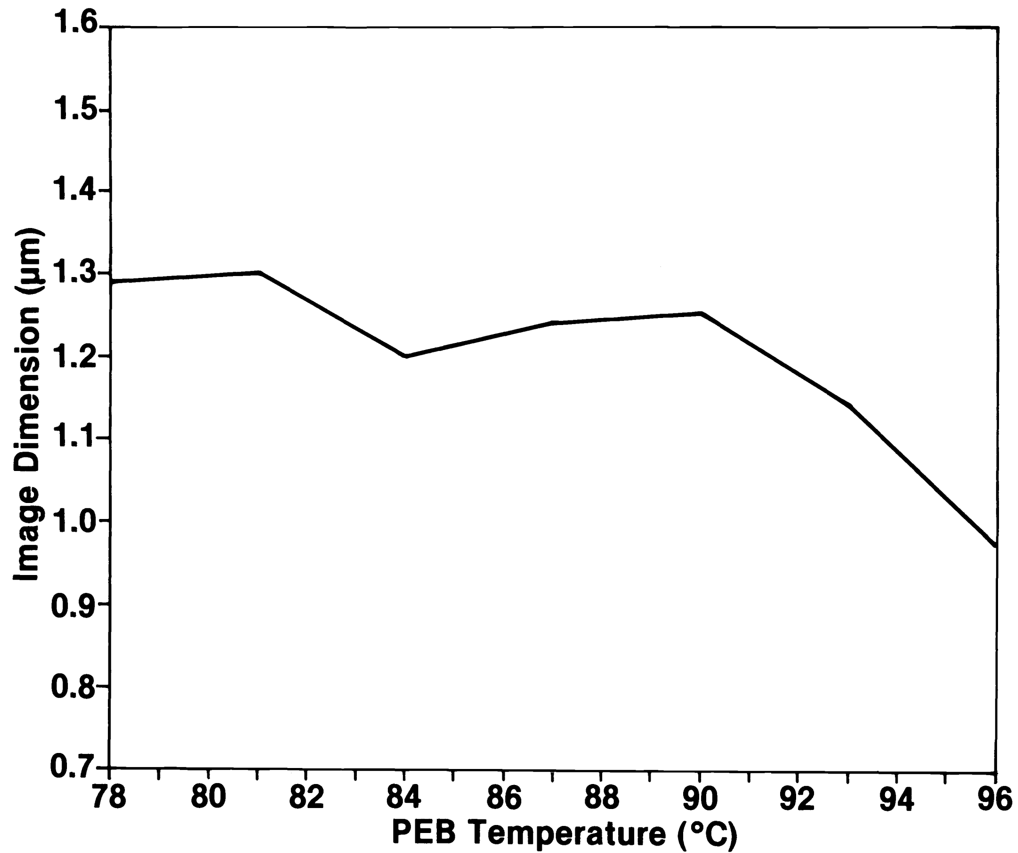


Figure 1. DUV resist image dimension vs PEB temperature

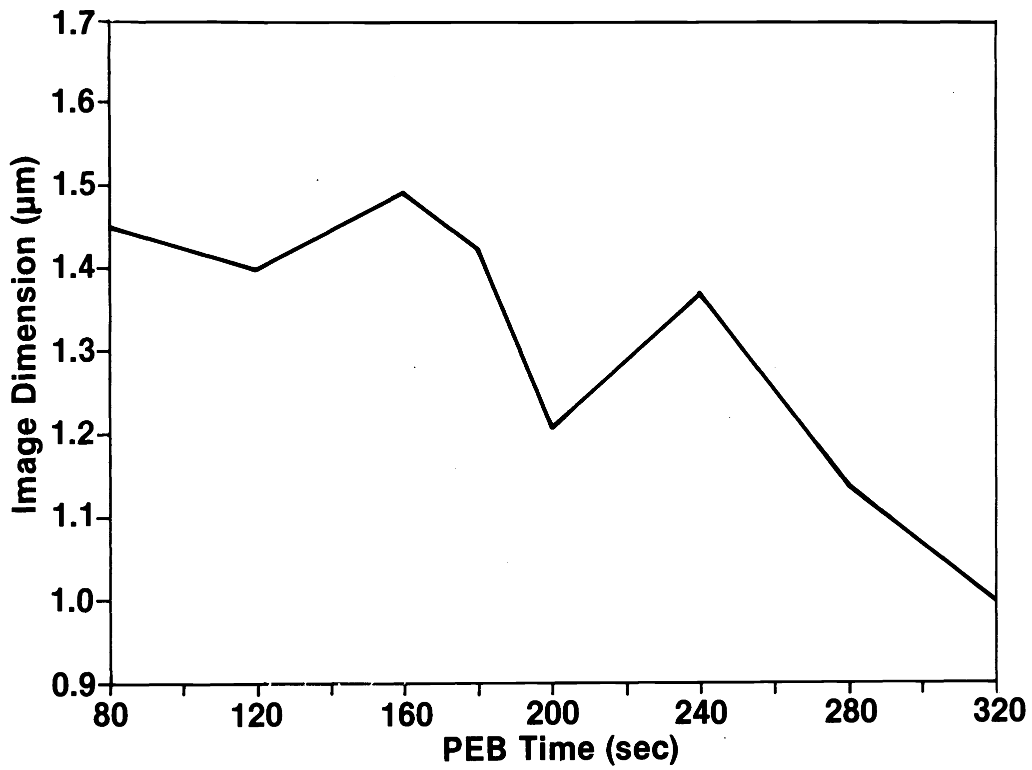


Figure 2. DUV resist image dimension vs PEB time

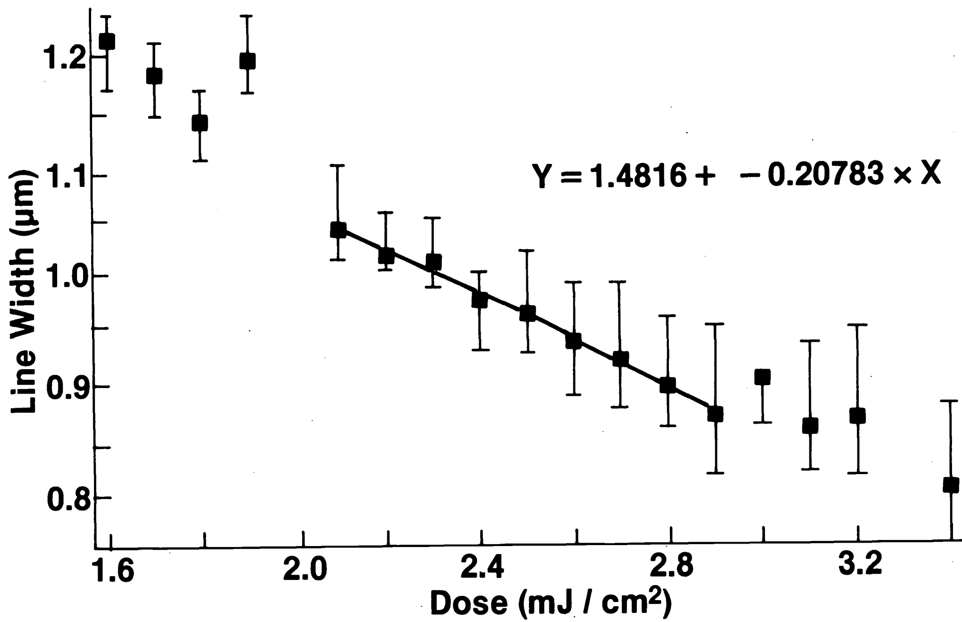
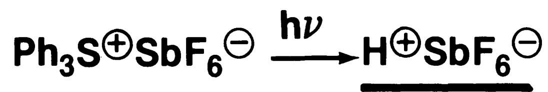


Figure 3. T-BOC line width dose curve



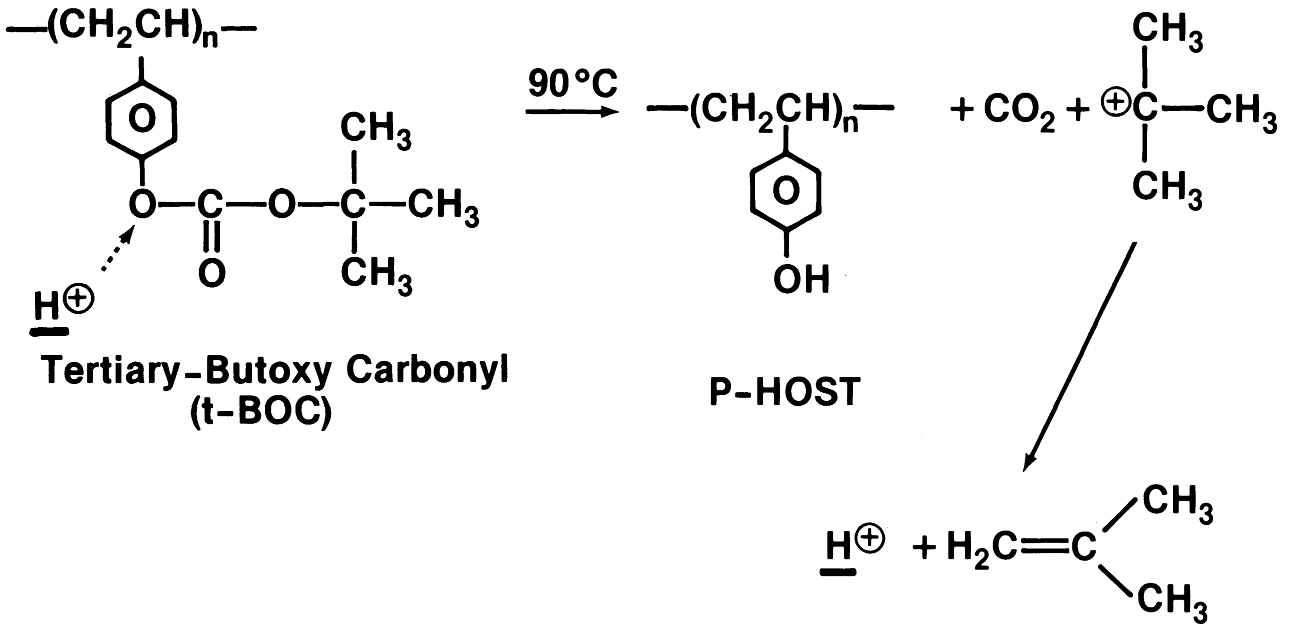


Figure 4. T-BOC image formation mechanism

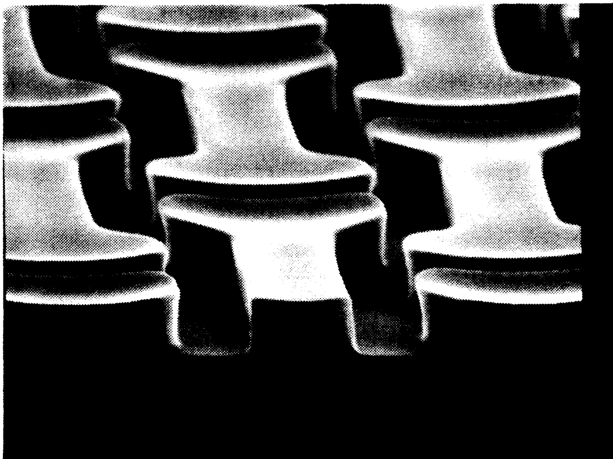


Figure 5. First-level isolation mask

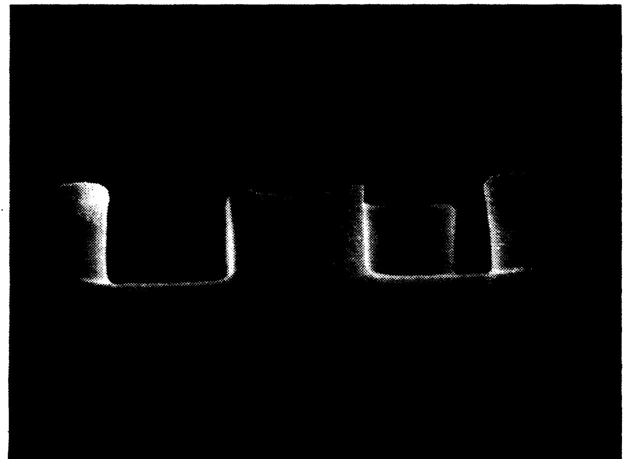


Figure 6. Cross-sectional view of first-level isolation mask