Metrology in times of shrinking budgets

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ABSTRACT

Variations in key device parameters such as gate width, fin height, and storage node aspect ratio can lead to performance variations device to device and within die. Extreme excursions can result in yield loss. Metrology and process control are enablers to detect and keep these variations to within certain bounds. As the features of devices continue to shrink, the allowable tolerances for critical dimensions and overlay errors likewise must shrink, in turn forcing the metrology budgets to shrink in step. At the same time, more data is required per wafer to generate higher order analyses while at the same time greater productivity in terms of silicon area processed in unit time is needed to keep the economics favorable. It is essential we develop the strategies needed for metrology in times of shrinking budgets.

Keywords: semiconductor metrology, CD and overlay, integrated metrology, process control

1. INTRODUCTION

Standalone metrology is the least appreciated module in the silicon device process. It is common to have the fab manager say, "I want that tool out of my area. It makes no wafers, stretches cycle times, and sits taking up expensive cleanroom space. It has no value."

Metrology sensors within the scanner such as focus and wafer leveling, and wafer alignment are rarely criticized as unnecessary. Largely this is due to their effectiveness, but also their relative invisibility and integration within the scanner itself. No floorspace is sacrificed. In the case of a dual stage scanner, very little time is actually sacrificed to the metrology measurements so cycle time is not impacted, a major breakthrough in productivity. It is natural then to look to a future in which metrology is integrated into lithography tools.

There is increasing demand on metrology as feature size scales. This requires metrology equipment to continue reduction of metrology gauge uncertainty. In addition, the metrology tool and process marker must be increasingly insensitive to process variations in films and wafer topography. Furthermore, the productivity must increase so that the metrology cost of ownership does not skyrocket.

The industry roadmap for minimum feature sizes in the major device types of NAND, DRAM, and logic are shown in Figure 1 where the data are from customers of ASML. We see the annual reduction of minimum half pitch is between 14 and 17% depending on device (Moore's Law is ~ 16% per year, or 30% every two years).

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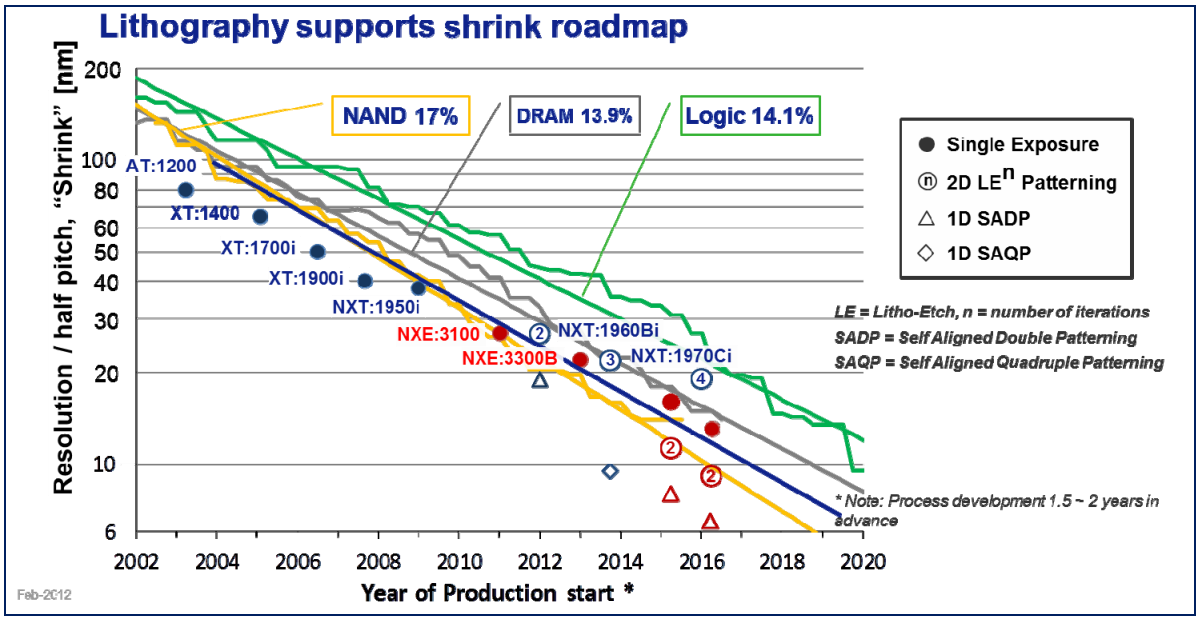

Figure 1: Industry roadmap towards <10nm resolution. Lithography supports the shrink roadmap.

The corresponding requirements for critical dimension uniformity (CDU) and overlay are shown in Figure 2. NAND is the most aggressive technology in terms of feature size scaling but microprocessor logic (MPU) requires the tightest CD control. DRAM is the most demanding technology for overlay. Focus control for immersion is nearly constant in the next few years due to the fact that we have reached the double patterning era and feature size reduction in ArFi is accomplished by LE^n or SADP type processes which start with a constant feature size printed by the scanner. Focus control requirements for EUV are falling and will soon shrink beyond what is needed in immersion with the advent of higher NA optics.

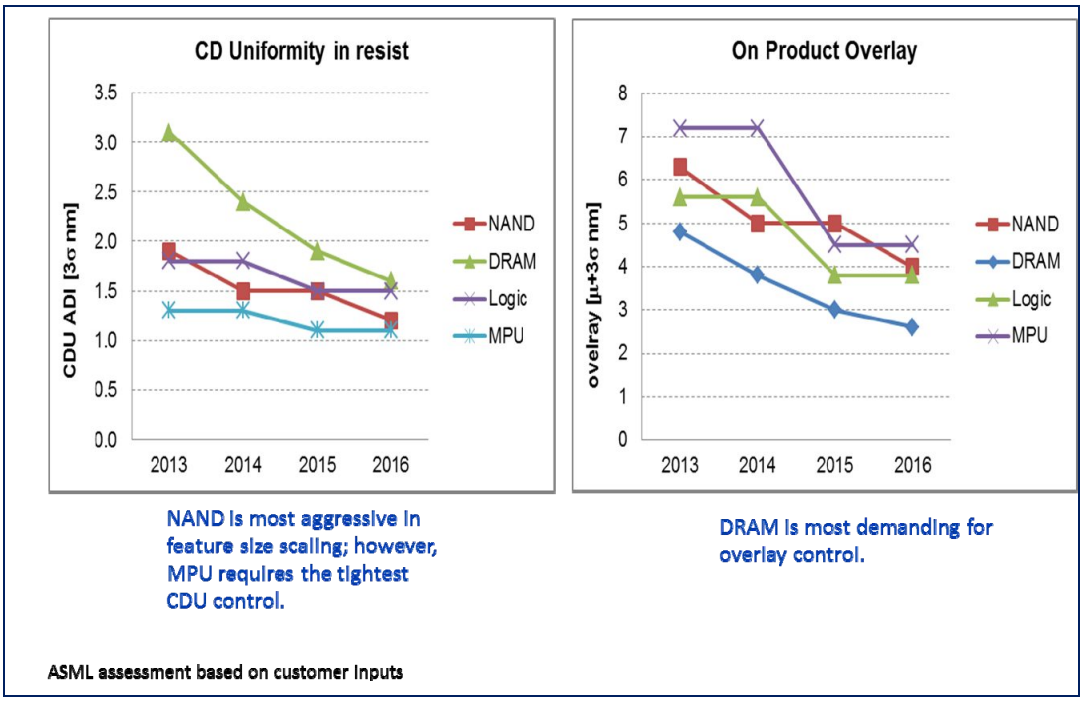

Figure 2: Estimated lithography process control requirements.

Following the gauge makers rule of metrology error can be no more than 10% of the minimum process error, Figure 3 shows the requirements for CD and overlay measurement error in nm. In double patterning cases such as litho-etch-litho-etch (LE^2), the overlay tolerance is even tighter [2] and requires a corresponding improvement in the gauge error.

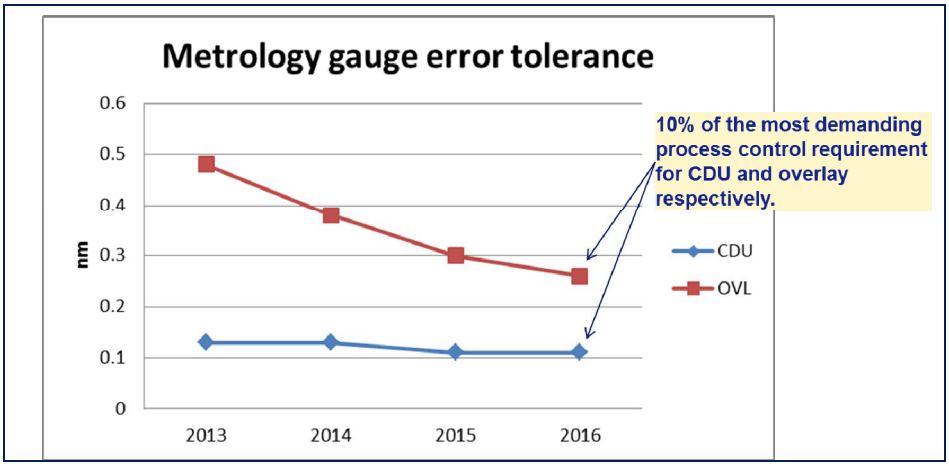

Figure 3: Metrology requirements in time of shrinking budgets.

2. SHORT HISTORY OF THE METROLOGY AND PROCESS CONTROL CONFERENCE

2.1 The Past 25 Years of the Metrology Conference

I will try to give my opinion on how this key conference came to be and how it has evolved. Probably my views are incomplete and wrong in some cases, but this is the way I remember it. The conference was started by Diana Nyyssonen and Mike Postek, both from the National Bureau of Standards (NBS, later renamed the National Institute if Science and Technology or NIST), and Kevin Monahan and Talat Hasan, then with Philips-Signetics. Papers presented in the Metrology Conference in the early 1990s dealt broadly with the measurement tools themselves and their characterization. How to inspect and measure micron and sub-µm level device features? What were the physical issues and what were the error budgets? Optical microscopy was used to measure both CDs and overlay. Scanning electron microscopy was starting to be introduced to FABs for CD metrology when feature sizes shrank below 1 µm. Electrical measurements were used to collect volumes of data on process overlay and final etched CD uniformity.

In the 2000s the emphasis shifted to using the tools to characterize and monitor semiconductor lithography processes and how to control them better. References [1-11] are the top downloaded papers from the Proceedings of SPIE in this Conference for the past 25 years, as supplied by the Director of Publications of SPIE [23]. The top paper [1] had more than 350 downloads as of the writing of this paper. Reading through these papers one can see 6 of 11 deal with scanner overlay, 2 deal with measurement of CDU from lithography, 1 deals with focus measurement of the scanner, 1 deals with optimizing the structure of the wafer target to measure scanner dose and overlay, and 1 with the forbidden pitch problem of optical proximity correction. This indicates the primary interest of readers of the conference proceedings, based on this metric of most downloads, is the characterization of scanner performance and its optimization.

In parallel to this, references [12-22] are the winning papers of the Diana Nyyssonen Award, given annually to the paper which is judged the best paper of the Conference by the members of the Program Committee [24]. These papers deal more specifically with the technologies developed to make measurements: 6 deal with scatterometry, and 4 with

CD SEM. While all papers [1-22] were written between 2001 and 2011, there is no paper on both lists. This is a puzzling fact, perhaps indicating a gap between what lithographers want to know and what the expert metrologists think are the key issues.

2.2 Metrology and Process Control for Scanners

One of the Nyyssonen Award winners [13] is representative of an important trend in how metrology and process control have evolved to support lithographic patterning, specifically to monitor and control the output of the scanner. Figure 4 shows the scheme for using a stand-alone scatterometry tool to monitor dose, focus, and overlay of a high NA immersion scanner.

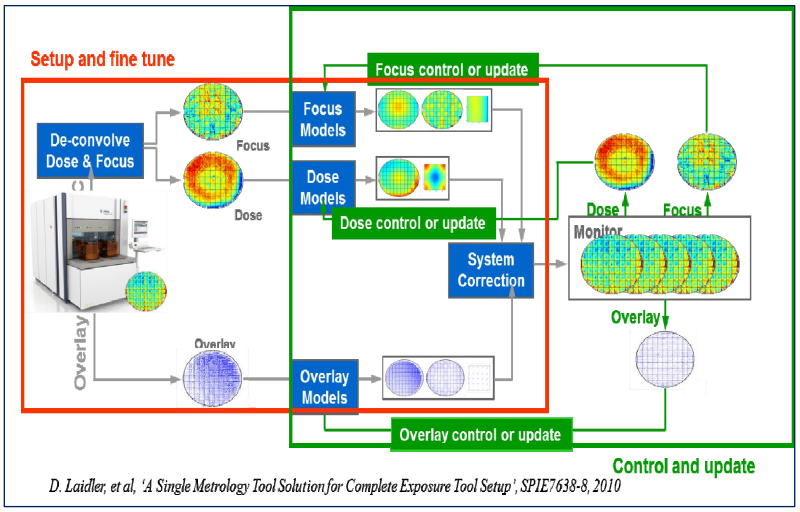

Figure 4: A single metrology tool solution for focus, dose and overlay scanner setup [13].

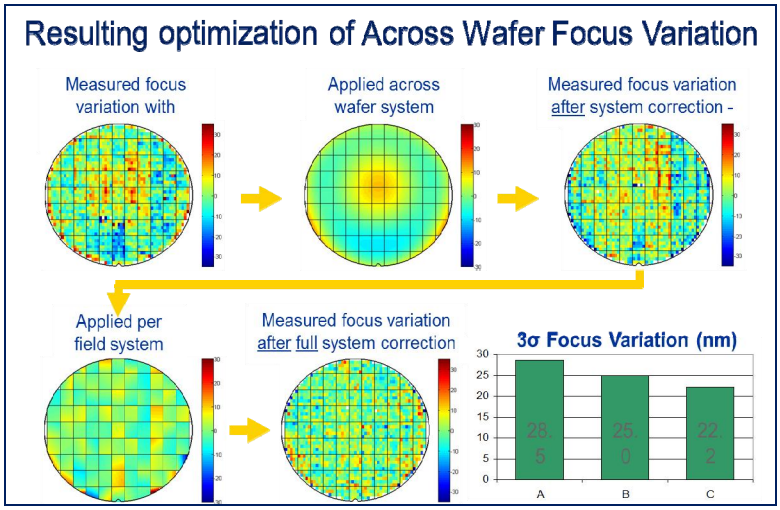

Figure 5: Resulting optimization of across wafer focus variation [13].

Figures 5 and 6 show the improvement possible in across wafer focus variation and across wafer overlay using this strategy for metrology and process control. Across wafer focus variation is improved from 28nm to 22nm, while across wafer overlay error is improved from almost 14nm to less than 4nm, substantial improvements in both parameters.

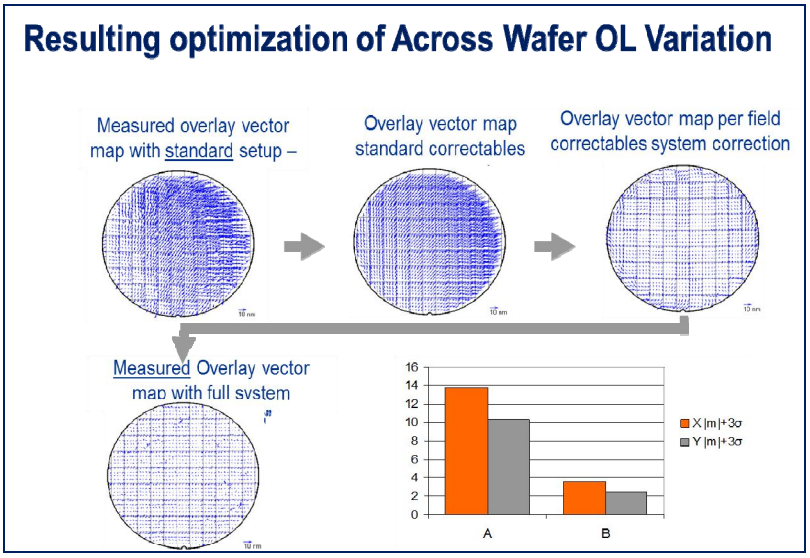

Figure 6: Resulting optimization of across wafer overlay variation [13].

3. THE PRESENT

3.1 Metrology and process control's role in supporting semiconductor lithography today

Metrology, inspection and process control are to the practitioners of the art of lithographic patterning, the basic eyes with which we judge how we make chips and correct our errors. After 25 years the field is vibrant and offers incredible capabilities in measurement, in defect detection and in methods to guide scanner lithography, the focus of this paper.

3.2 Dose, focus, and overlay control in scanners

Dose and focus are the primary scanner knobs available to a lithographer to control the size and shape of the device image in resist. Of course resist chemists and track engineers play a key role but they must write their own history. In lithography there are many classic papers which describe the intense interplay between dose and focus [25-29], but a great work for workers in metrology to start with is [30].

Nanometer scale overlay in scanners is probably the key achievement of lithography. Many papers describe the outstanding resolution achieved by various techniques (multiple direct write e-beam [31], nano-imprint [32], DSA [33], scanning probe [34]) but what about the data on how a full chip can be overlaid with a previous device layer? The published data falls well-short of the device requirement shown in Figure 2. This is the most complex subject of lithography, dealing with aligning mask features to wafer features, through diffraction limited optical systems.

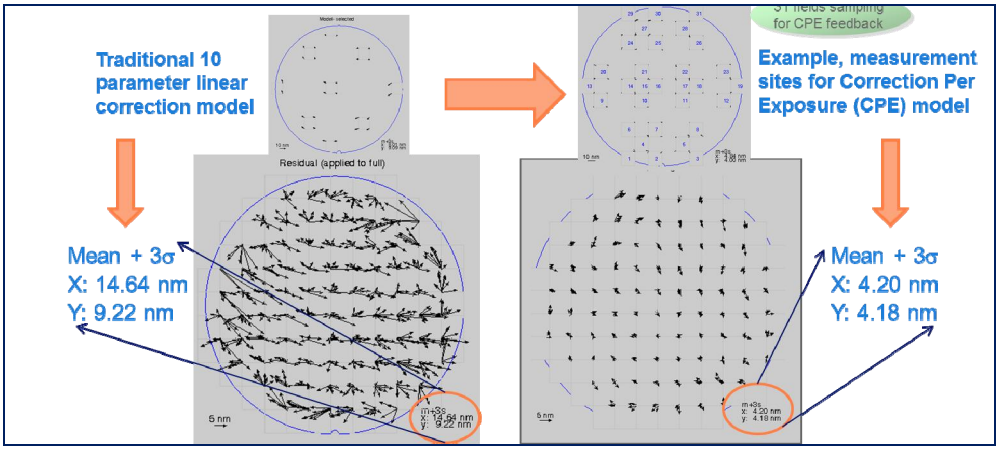

Figure 7: Higher order overlay correction model requires additional measurements.

Simple but effective low order overlay models were developed in the 1970 and 80's [34, 35] to describe the errors of reduction steppers and 1x projection scanners. Higher order process corrections and corrections per exposure have been employed in the newest scanners to reduce on-product overlay errors to less than 5nm (Figure 7). This is accomplished by measuring overlay targets in scribe lanes (Figure 8), large but well-chosen sampling plans and using corrections made in every exposure (Figure 9).

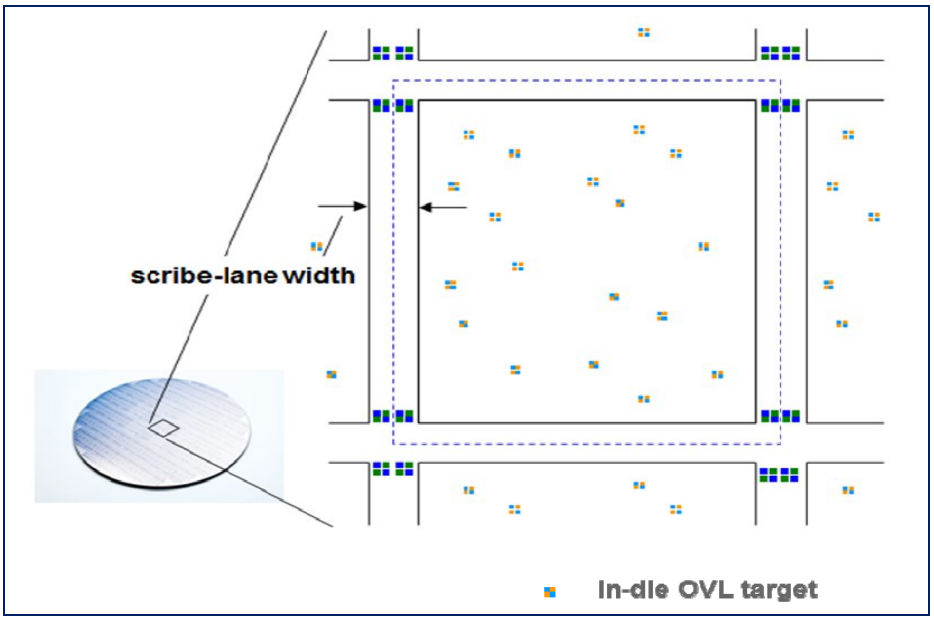

Figure 8: IC makers request additional intrafield overlay information.

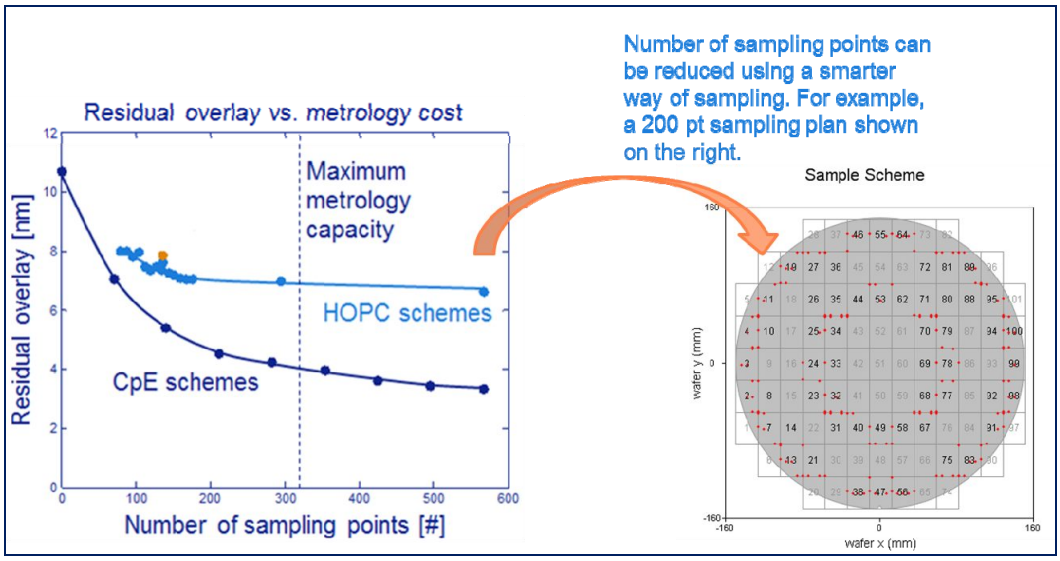

Figure 9: Overlay improvement is enabled through increased sampling and corrections per exposure.

Finally, integration of the metrology tool within the lithocell enables tight process control loops and rapid stabilization of overlay and focus on product wafers, see Figure 10 (after [37]).

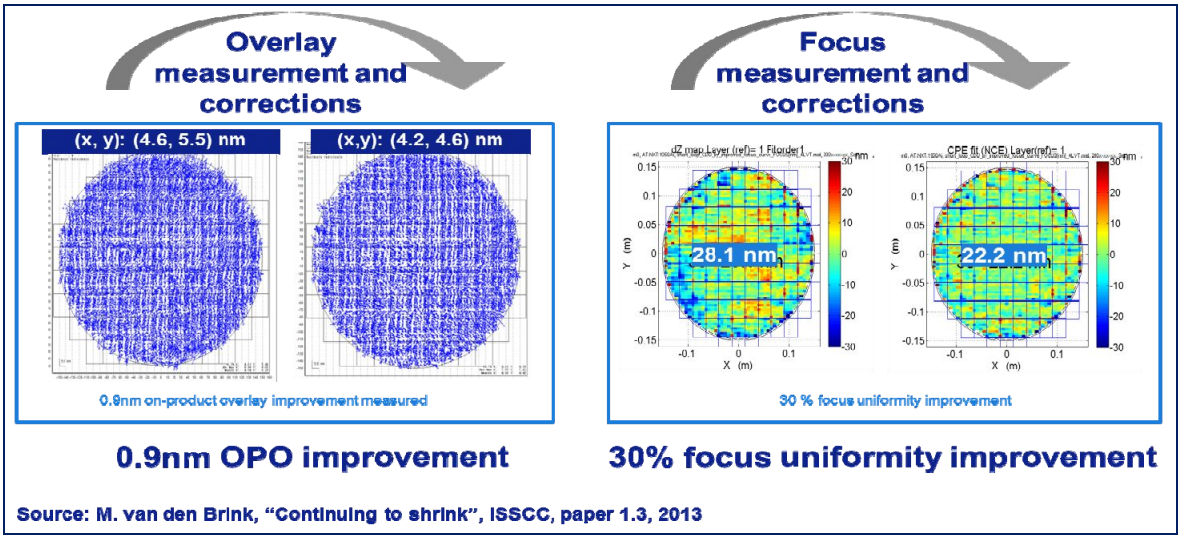

Figure 10: Integrated metrology can improve on-product overlay and focus.

4. THE FUTURE

4.1 Some grand challenges for the future

In this section I will mention a few outstanding problems for metrology and process control going forward. First, support new, smaller device structures with metrology. New device structures are expected as memories and logic devices continue to shrink. The main trends are the continuing extension of planar floating gate in NAND but also the industry is moving to various 3D device concepts with relaxation of half pitch [38]. Metrology challenges for high aspect ratio etching loom. DRAM is expected to extend its $6F^2$ cell layout path. DRAM has long depended on high aspect ratio structures for its capacitors. Foundry is moving to FinFETs and away from planar transistors. FinFETs are likewise 3D devices which stick up above the wafer topography.

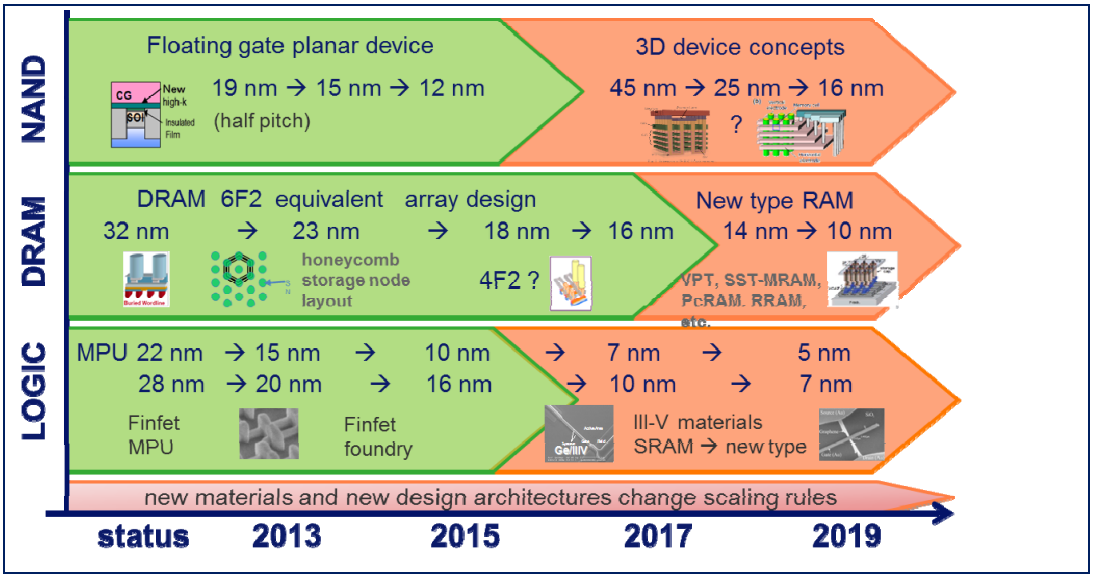

Figure 11: Device scaling assumptions as input for lithography solutions.

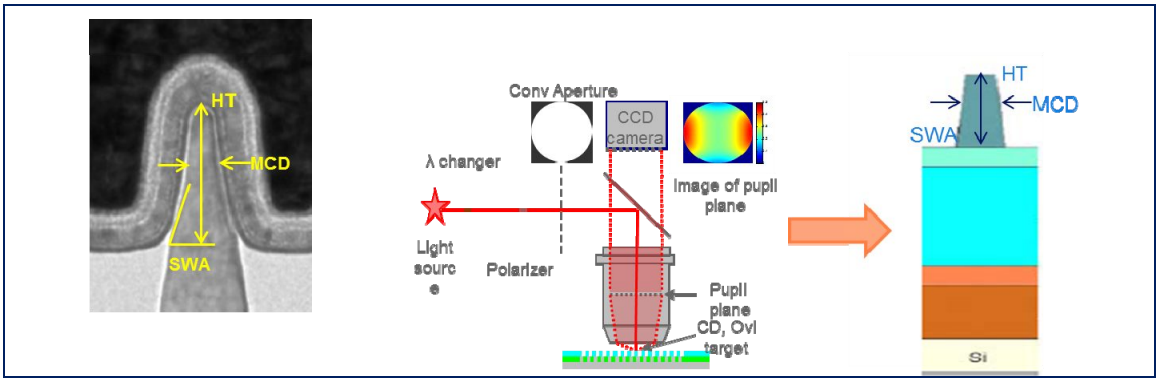

Figure 12: How to support the needs of new device structures? FinFET transistors need profile and height control in addition to CD [42].

The 3D FinFET transistor requires extra metrology to control height and profile of fins in addition to its CD. Can scatterometry meet this challenge? Today's approaches to solution for this challenge are found in one of Diana Nyyssonen Memorial Award winning papers [15] and in the more recent work, such as [42] illustrated n Figure 12.

A second grand challenge is to devise metrology and process control loops which can correct variation mid-process and, in effect, add back information that is lost during the patterning process.

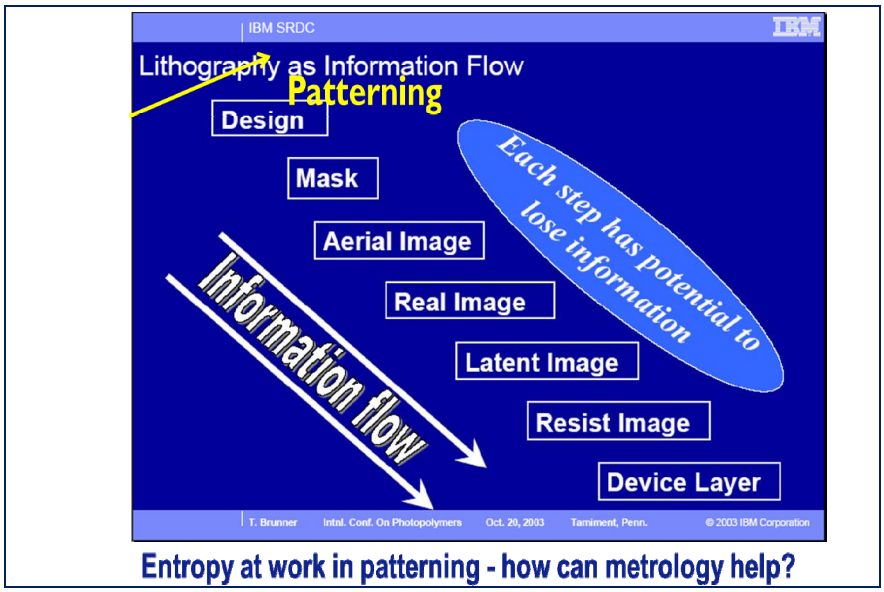

Figure 13: Information Flow from Design to Device [39].

Figure 13 from Tim Brunner [39] illustrates the lithographic patterning flow and makes the point that each step in the process has the potential to lose information. For example, electron beam patterning of the mask results in variances from the GDS in CD and pattern placement. Further, high frequency information from the mask is not passed by the optical system, resulting in rounded corners of features or round contacts.

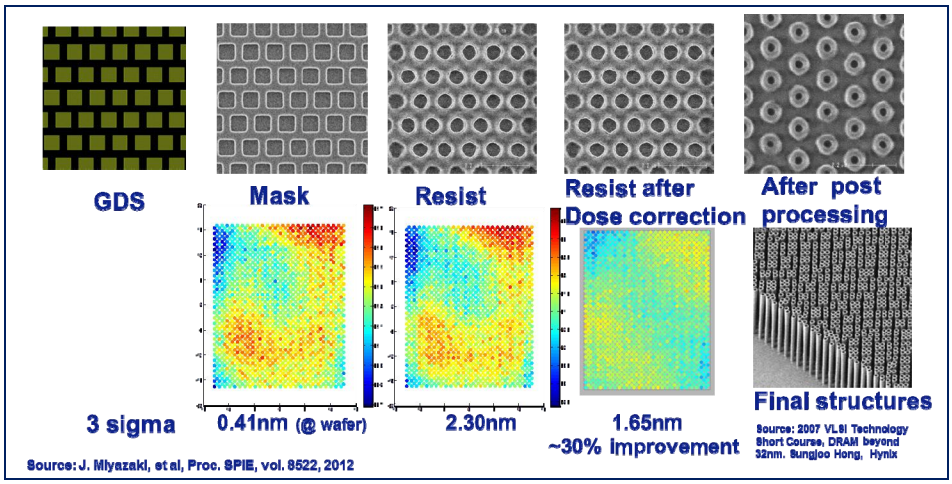

Figure 14: How to create processes which correct variation mid-process and in effect add information back which is lost? [40].

Can we perfect the patterning flow using metrology and process control loops which reduce initial image variation from the mask and scanner through scanner control mechanisms such as dose correction and through resist post-processing (e.g. directed self-assembly for via healing)? See Figure 14. The role of metrology and process control is more than measurement of CDs and overlay - it is ultimately to realize the design intent and enable complex device structures.

A final grand challenge is to measure structures much less than λ/NA in size with optics. This is effectively done in optical scatterometry but more improvement is required to solve the general problem of measurement of dense wafer features on typical CMOS thin-film stacks.

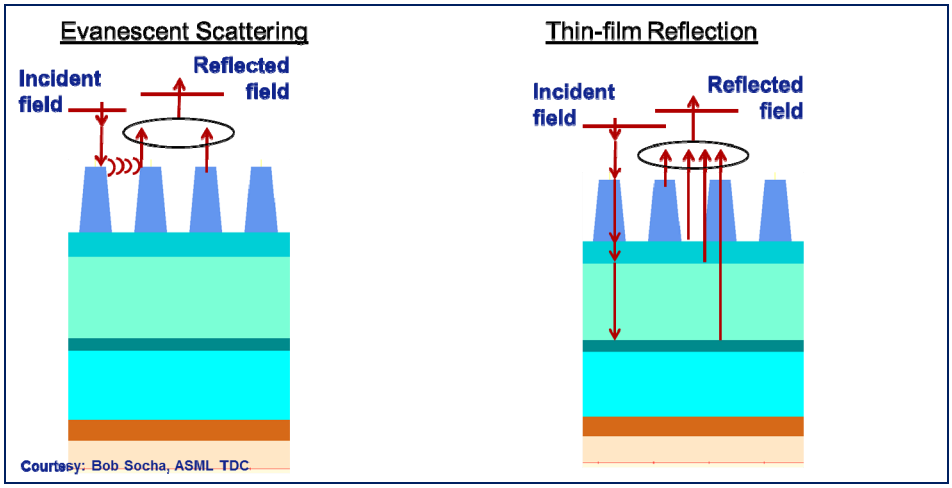

Figure 15: How to measure features much smaller than λ/NA with optics? Evanescent scattering and thin film reflection phenomena in scatterometry [41].

Let us consider the problem of measuring such features with optical or DUV scatterometry [41]. Scattering from feature edges creates evanescent fields which adds or subtracts from zero order reflection. The reflected signal is a summation of all the reflections from the pattern and thin-film stack. A strategy may be to choose a wavelength (and/or angle of incidence) to increase the evanescent effect but to reduce the thin-film reflection. The evanescent field effect is often small. The zero order reflection from the patterned area dominates. The zero order reflection from the patterned area is proportional to the volume of the feature, whether the feature itself varies in height, width or sidewall angle. Consequently knowing the typical variation in a process is important. For example, the resist loss of a trapezoid may be too much for a well categorized manufacturing process. This possibility is eliminated through a constraint. The better one understands the process variability, the better the scatterometry results. While it is remarkable what we can do with light, what more can be done?

5. CONCLUSION

Metrology and process control are for a long time enablers of lithography for semiconductor production. High speed integrated metrology based on scatterometry has successfully entered mainstream production for overlay, focus, and dose monitoring of scanners. Grand challenges in supporting new device types, in adding back information that is lost in patterning, and in measuring features much smaller than the wavelength with optics give us much more to do as the future unfolds.

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