

Teaching and research in integrated microelectronics

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ABSTRACT

In this paper we present a concept to train physics students in the field of integrated sensor design realized at the faculty of physics and astronomy at Heidelberg University (Germany). A laboratory for design and test of integrated sensor chips has been set up and a course program for physics students has been introduced. The work of the laboratory is illustrated by the presentation of a project to design and build a tactile vision substitution system based on so-called *vision chips*.

Keywords: microelectronics, physics, sensors, teaching, ASIC, CMOS, vision chips, image processing, TVSS

1. INTRODUCTION

The teaching of physics students traditionally follows a standard curriculum involving all fields of classical and modern physics. Theoretical concepts as well as experimental approaches are part of the lecture program. Typically 10 – 20% of the students later end up in basic physics research. The majority however takes positions in industry, where they have to compete with computer scientists and engineers. In this paper we argue that the excellent knowledge of physics concepts forms an ideal basis for the development of integrated sensors for physical quantities like light, temperature, radioactivity and alike. Here integration means the combination of the detection element (sensor) and analog and digital signal processing on one custom made silicon ASIC (*Application Specific Integrated Circuit*) chip. These so-called mixed-signal sensor chips will become increasingly important for our daily life. The car industry is already employing a multitude of sensors to gain information about the status, the position and the movement of the vehicle. So-called *vision chips* are good examples for rather complex light sensor systems with integrated intelligence for image processing.

If we accept the need for such devices it is evident that universities have to offer appropriate training to students in related areas. Physics students are well trained in classical physics (e.g. electrodynamics) and in modern fields of physics like quantum mechanics and solid state physics. A proficient understanding of these fields is essential for the design of integrated sensors. What is missing in most physics faculties are dedicated course programs and laboratories for integrated microelectronics.

The faculty of physics and astronomy at Heidelberg University (Germany) has in the recent years built up a concept of lectures and laboratories in this field. In this paper we will present the project and one particular example of a research activity carried out there.

2. THE HEIDELBERG ASIC LABORATORY FOR INTEGRATED MICROELECTRONICS

The faculty of physics and astronomy in Heidelberg (Germany) has build up a laboratory dedicated to microelectronics and sensor development. In this chapter we will describe the structure and the research program of this *ASIC laboratory for microelectronics* as well as the related training activities for physics students in Heidelberg.

1. Structure and Research Program of the ASIC laboratory

Working with ASIC chips in a university laboratory with limited financial resources requires external support for chip production and for the purchase of the very large and complex software packages used for CAD, simulation and synthesis. The EURO PRACTICE program offered to academic institutions by the European Community has been crucial in the foundation process of the Heidelberg ASIC laboratory. The purchase of the software package CADENCE as well as various

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ASIC production runs carried out at European chip foundries have been subsidized through this program. The basic infrastructure is acquired and maintained as a pool to which all users in the faculty and beyond (Max-Planck Institute) contribute. Expensive devices like waferprobers, bonders and high performance computing facilities are hence affordable and can be used efficiently.

The lab is structured into a design and a test department. The design department provides users with support for the CADENCE chip design package, technology specific databases and various related software packages. An overview of the infrastructure available in the design department can be found in table 1.

Hardware	Hewlett-Packard PA-RISC Workstations 9 Workstations, 20 Color CAD consoles 15 SUN-SPARC Workstations for Teaching
Software	CADENCE Design Framework (Schematic Entry, Simulation, Layout Editor, Design Rule Checker, Layout versus Schematics, Verilog HDL, VHDL, Router + Placer, Allegro PCB Layout + Simulation, MCM Layout + Simulation) SYNOPSYS Synthesis HSPICE Simulation SILVACO Virtual Wafer Fab (Device Simulation) XLINX, ALTERA FPGA Software

Table 1: Hardware and software infrastructure of the Heidelberg ASIC laboratory (design department).

The test department provides facilities for testing and handling of bare chip dies, packaged chips, MCM's (multi-chip-modules) and printed circuit boards. Major pieces of equipment in this part of the laboratory include a semiautomatic wafer prober for serial testing of wafers, a fast HP82000 chip-tester and facilities for handling and connecting of bare chip dies. For the development of optical sensors (see next chapter) an optical laboratory with programmable light sources and precision scanners is available. Table 2 gives an overview of the infrastructure in the test department.

Electronics Testing	HP82000 Solid State Circuit Test System (400 MHz) Analog and Digital Oscilloscopes Arbitrary Function Generators Spectrum Analyzer Standard Electronics Lab Equipment
Die/Wafer/Board Handling	Manual Wafer Prober Semiautomatic Wafer Prober Wedge-Wedge Bonder Microscopes Laminar-Flow Workbenches Temperature Box Printed Circuit Board Production Facility
Optical Testing	Optical Table Programmable Light Sources Precision x-y Scanner
Instrument Control	HPIB (IEEE 488) Instrument Control HP-VEE (Visual Electrical Engineering) VME Systems LabView

Table 2: Infrastructure of the Heidelberg ASIC laboratory (test department).

The research program carried out in the ASIC laboratory is determined by the projects of the contributing institutes. Initially founded to produce microelectronics for experiments in experimental particle physics the laboratory has since then expanded its scope towards medical physics and cooperation with medium-sized companies for knowledge transfer.

The applications in experimental particle physics do mainly deal with the readout of multi-channel detectors for ionizing radiation. These detectors liberate very small electrical charges which have to be converted with low noise into measurable voltage signals which in turn need to be processed by digital signal processors to find pre-defined patterns in very short time (typically ns to μ s scale). The medical physics projects of the lab are carried out in cooperation with the Heidelberg Eye Clinic. Two projects are currently under way. One is the development of a Hartmann-Shack Sensor for wavefront analysis in real time. The ophthalmological application is the development of a retina scan tomograph for morphological studies of the human retina. The other medical physics project is the development of a 'Tactile Vision Substitution System (TVSS)' based on an intelligent image sensor (Vision Chip). This project is described in the following chapter.

Cooperation with industry is carried out with support from the European Community for so-called *First Users*. The idea is to use the facilities for teaching and research available at universities to bring modern technology to small and medium sized companies, which would otherwise not be able to afford specialized staff and equipment in this field. The Heidelberg laboratory has developed a precision quartz oscillator with temperature compensation. This project is a good example for integrated sensor concepts because it combines the temperature measurement, analog and digital data processing on one silicon chip.

2. Training Program for Physics Students

As already mentioned in the introduction, the normal course of study for physics student does not include any particular training in microelectronics. For those students interested to proceed into this field, the faculty of physics and astronomy in Heidelberg offers a series of specialized lectures. The contents of those lectures have an increasing degree of specialization. In the first or second year essentially all students receive an introduction into technical computer science. This lecture and the associated exercises are an essential prerequisite for experimental work in any science today. The next step is an introduction into conventional electronics containing technologies of sensors and optoelectronics. Here a laboratory class is offered in addition to gain first experience with circuit design, building and de-bugging as well as with the operation of modern laboratory equipment. Each student has to his disposal a personal computer, a fast oscilloscope, a logic analyzer, an arbitrary waveform generator, a programmable power supply and a collection of electronics components.

Lecture	Topics	h/week	year
Technical Computer Science	Logic networks, computer architecture (register, data paths, assembler programming, pipelining, caches, memory hierarchies, input/output, arithmetic, performance, buses), networks, operating systems.	4	1 st or 2 nd
Exercises related to the above	Programming exercises and computer hardware related exercises	2	1 st or 2 nd
Electronics	Electronic components, basic analog circuits, feedback circuits, signal transmission, optoelectronics, sensors, digital circuits and systems, signal processing and data acquisition	4	3 rd or 4 th
Laboratory Work related to the above	Design, realization and test of electronics circuits	2	3 rd or 4 th
Introduction to ASIC Design	Introduction to integrated circuit technologies, production of integrated circuits, MOS transistors, bipolar transistors, components in CMOS circuits, simulation techniques, design of CMOS circuits, example of an operational amplifier, layout techniques, hardware description languages, synthesis, programmable logic arrays, test devices	2	4 th
Circuit design workshop	Circuit analysis techniques, ASIC layout techniques	2	5 th

Table 3: Optional lecture and laboratory class program associated with microelectronics at the faculty of physics and astronomy in Heidelberg

Before entering one of the research groups for a thesis work the students have the choice to attend a special lecture on ASIC design. Here the tools of chip design are introduced so that the students receive a good preparation for their own work in

this field. If the student chooses to work in the ASIC laboratory he will receive continuous training on the most recent developments in microelectronics by joining the so-called *circuit design workshop* carried out on a regular basis in the laboratory. Table 3 presents an overview of the training program. Experience has shown that students joining the research groups are well prepared and ready to make useful contributions to the actual projects.

3. AN EXAMPLE OF A RESEARCH PROJECT (TACTILE VISION SUBSTITUTION)

In this chapter we present one particular example of a research project carried out in the lab. The project involves the development of an intelligent image sensor (vision chip).

Vision substitution systems with tactile displays have been successfully employed for the first time by Bach-y-Rita and Collins.¹ Despite their principal success practical applications have been hindered by the fact that the two basic components, image acquisition and tactile display have been rather clumsy thus excluding portable devices. In the meantime technology has advanced in particular in the areas of microelectronics and high performance computing. The first area allows us to design highly compact photodetector arrays with specifications similar to the front-end of the human visual system (*vision chips*). The second area makes it possible to read out and process digital data in real time. Using these technologies together with a tactile display unit we have developed, built and tested a *Tactile Vision Substitution System (TVSS)* which gives blind people access to the real visual world as well as to computer graphics, drawings and similar artificial patterns.

Basically the TVSS system developed in Heidelberg is based on a dedicated vision chip to capture and process the image, a conventional laptop PC to control the hardware units and to carry out further image processing and a tactile output device. In the following we will focus on the vision chip. Details of the complete system can be found in ².

The vision chip is a single chip camera system designed and built using standard *Complementary Metal Oxide Semiconductor* (short : CMOS) technology. The availability of basic circuit elements like diodes and transistors suggests to use the intrinsic photoelectric effect in the depletion zones of CMOS pn-structures for light detection. At the same time the possibilities for further signal processing on the same silicon wafer can be used. This is the basic idea of CMOS photoreceptors (*vision chips*). Apart from the integration of sensor elements and signal processing CMOS photoreceptors are characterized by a huge dynamic range of 1 : 1 million or more. This performance comes close to the biological model and is far better than that of conventional CCD systems. This is of great advantage for the application in mind, because such a system can operate under a large range of different illuminations without the need for additional aperture corrections which would require additional space and electrical power. In practical applications however, the use of the large dynamic range is difficult. A linear transfer of many orders of magnitude in incident illumination requires an unrealistic range of output voltages. A way to overcome this problem also realized in biological systems is a logarithmic compression of the electrical output signal. Two types of logarithmic response camera systems with different specifications have been produced in the ASIC laboratory at the faculty of physics and astronomy at Heidelberg University.

The first system type is based on the 1.2 μm CMOS technology of the company AMS (Austria Micro Systems). This CMOS process offers two metal and two polysilicon layers. The system uses the adaptive pixel concept ³ with logarithmic response to the incident light intensity and has been developed in the initial phase of the Heidelberg vision project. Detailed measurements have been performed with this camera system describing in particular the phototransduction mechanism characterizing the specific CMOS process ⁴.

All CMOS *vision chips* have to cope with the problem of mismatch between individual pixels. This well known effect is called "fixed pattern noise" and poses a considerable problem for subsequent image processing since it generates artificial local contrasts which are easily detected by edge detection filters. The consequence for the tactile output is severe because the limited bandwidth of the somatosensory system would be overloaded with faulty information. The fixed pattern noise is a feature specific to CMOS based image sensors and currently represents one of their major disadvantages. The reason for this spatial noise can be allocated in the mismatch of individual transistors used for analog preprocessing of pixel data. In principle the effect can be reduced by increasing the size of the relevant transistors. However, this would increase the geometrical size of the individual pixels and in turn the size of the entire sensor above acceptable limits. The only practical way to handle fixed pattern noise is to apply a calibration procedure. Measurements carried out with logarithmic response pixels in the framework of this project show that the fixed pattern noise is dominated by offsets of the logarithmic response curves which can correspond to as much as 2-3 orders of magnitude in incident light intensity. The pixel-to-pixel variations of logarithmic slopes are usually negligible. Various methods for offset calibration have been proposed and implemented. The most obvious way is to use external frame memories or software methods. The required post-production calibration

procedure and the need for external components and databases are disadvantages, which do partly compensate some of the major advantages of CMOS sensors, their compactness and low price. On-Chip solutions like floating-gate technologies or hot carrier degradation⁵ as well need post-production calibration procedures, which in addition can take several hours for one chip.

Motivated by the need of a logarithmic sensor with small fixed pattern noise the Heidelberg group has developed a vision chip with a built-in analog fixed pattern noise correction. The chip is based on a continuously working photoreceptor with logarithmic response covering a dynamic range of more than 6 decades in incident light intensity. To calibrate the chip the system has to be brought into a reference state that corresponds to a defined sensor input. For that purpose all photoreceptors can be stimulated by the same reference current in a dedicated calibration cycle. Without fixed pattern noise all pixel outputs would show the same output signal. In reality the signals differ due to the problem described above. A differential amplifier compares individual outputs to the reference and adjusts each pixel until both signals are equal. The calibration is then stored in an analog memory available for each individual photoreceptor. Subsequent lines of pixels are being calibrated so that one differential amplifier per pixel column has to be implemented. The amplifiers are realized as auto-zeroing operational amplifiers in order to suppress column-by-column variations caused by the differential amplifiers themselves. The prototype chip features 4096 pixels arranged in a matrix of 64 rows and 64 columns. The architecture of the chip is shown in figure 1.

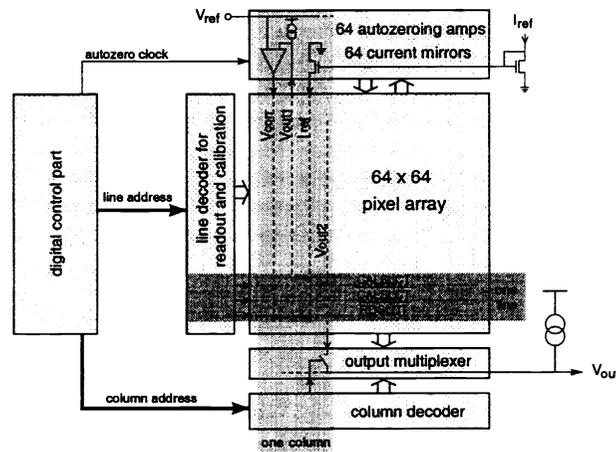


Figure 1: Architecture of the Vision Chip

The chip was fabricated in the 0.8 μm CMOS technology of the company AMS (Austria Micro Systems). This CMOS process offers two metal layers and two polysilicon layers like the one described above. A single pixel has an area of 33 μm x 33 μm . In total the chip has an area of 3.5 mm x 2.5 mm. The layout of the chip is shown in figure 2.

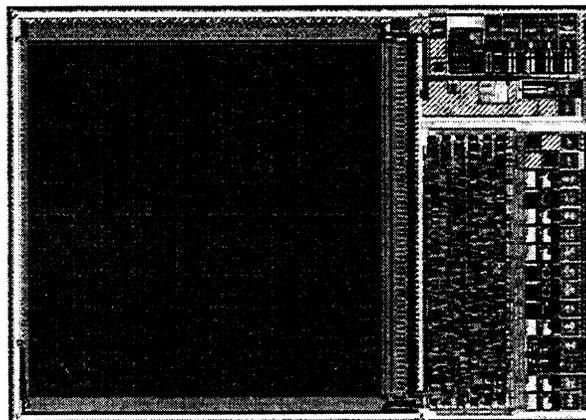


Figure 2: Layout of the Vision Chip

Measurements carried out with the produced chip have confirmed the expected behavior. The chip can safely operate over 6 orders of magnitude in incident illumination with an almost perfect logarithmic response. Figure 3 shows the measured response curve for a pixel on the chip. The slope is negative with an absolute value of 110 mV per decade.

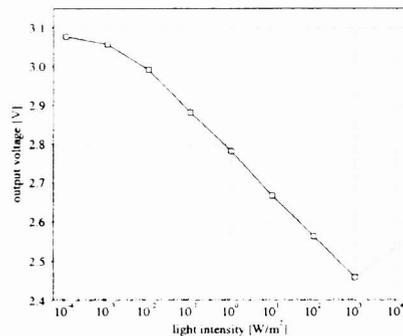


Figure 3: Pixel response measured over 8 decades of incident light intensity. The horizontal scale is logarithmic.

The other key feature of the chip is the analog self calibration mechanism. At a given uniform illumination the fixed pattern noise has a standard deviation of about 2 mV corresponding to a few percent of one decade in illumination. This has to be compared to the typical performance of uncalibrated CMOS vision sensors where fixed pattern noise corresponding to 2-3 decades in illumination has been observed which makes external calibration mandatory. Figure 4 demonstrates the performance of the fixed pattern noise correction by comparing the images of low contrast (one magnitude in illumination) rings with and without calibration. Details on the self-calibrating CMOS vision chip can be found in ⁶.

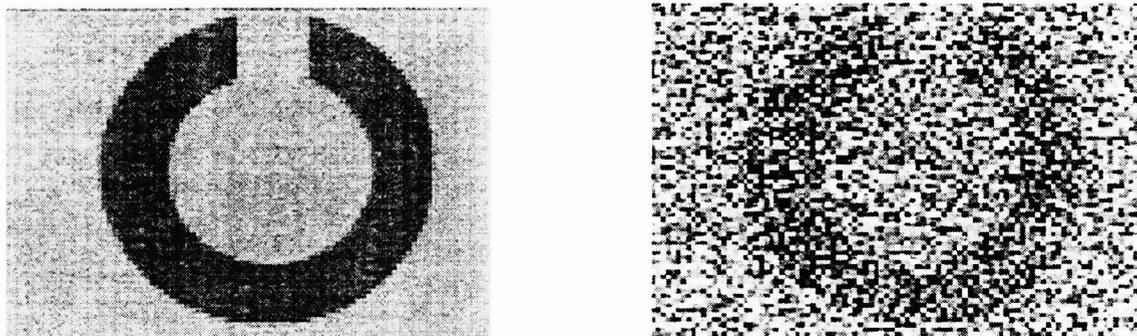


Figure 4: Low contrast (one magnitude in illumination) ring images with (left) and without (right) analog self-calibration of the fixed pattern noise.

4. CONCLUSIONS

The concept of introducing physics students to the design of integrated microelectronics and the integration of sensors for physical quantities in particular has been very successful. A variety of rather multidisciplinary research project has evolved at the university. Those students leaving the university are enjoying a collection of attractive job offers because there is a very high demand for physicists trained in this field. First examples for start-up companies brought into existence by former students from the lab are evolving.

ACKNOWLEDGEMENTS

This work was supported by the Ministerium für Wissenschaft, Forschung und Kunst des Landes Baden-Württemberg, Stuttgart (Germany) in the framework of the Landesforschungsförderung, by the Bundesministerium für Bildung und Forschung, Bonn (Germany) under contract numbers 05 6HD271, 05 5HA8VH1, 05 7HD28P, 05 7HD27P and by the European Community under contract FUSE 1812. The author wishes to thank Paul Bach-y-Rita for the invitation to this inspiring meeting and for the constant encouragement to perform interdisciplinary research work.

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