# Photomask and lithography technologies: Past 10 years and what will come next

Koichiro Hoh\*
The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo, Japan 113-8656
Organizing Committee Chair, Photomask Japan 2003

#### **ABSTRACT**

On the occasion of 10th conference of Photomask Japan, the advancement of this conference in the past decade is briefly reviewed and some emerging technologies related to lithography are discussed with examples. **Keywords:** Photomask Japan, participants and paper statistics, MEMS, CMOS gigahertz communication circuits, distortion correction of x-ray mask.

### 1. TEN YEARS OF PHOTOMASK JAPAN

Photomask Japan celebrates its 10th conference in April 2003. The first conference was held in April 1994 at Kawasaki city, Kanagawa Prefecture, Japan and 10 years has passed since the start of the preparation for the first conference. On this occasion I would like to express my sincere thanks to SPIE, BACUS and related people who have collaborated and supported all through this decade to make this conference successful.

Figures 1 and 2 show the statistics of the numbers of participants and presented papers for these ten years. Almost steady increase of participants and papers prove the significance of this conference. Numbers 400 to 500 of participants are certainly remarkable in Japan for the conference of this kind of technological area. Also notable is a steady increase of foreign participants and papers, which manifests that this conference is highly evaluated from abroad and is established as an international conference. These also prove that the scope of this conference always matches to the practical interests of related industries, not only in Japan but also in the world.

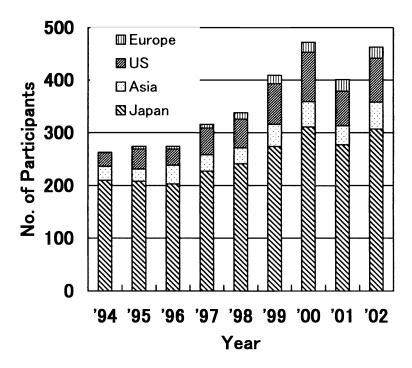


Fig.1. Annual change of the number of participants.

<sup>\*</sup> hoh@ee.t.u-tokyo.ac.jp; phone 81 3 5841-6675; fax 81 3 5841-4995

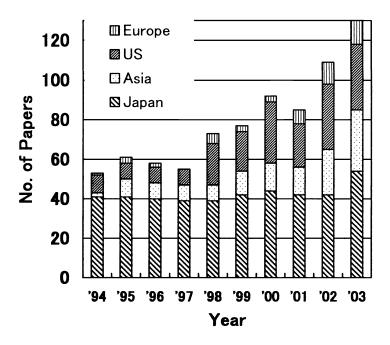


Fig. 2. Annual change of the number of presented papers.

#### 2. PHOTOMASK AND LITHOGRAPHY IN THE NEXT DECADE

During the previous decade of Photomask Japan, VLSI industry has experienced considerable changes. Fabs have scattered globally and reorganization or new alliances of traditional companies have been settled. In Japan we have several problems of our own. Although these situations exercise influence upon entire VLSI technologies, it seems that lithography still contains plenty of alternatives to be selected for pushing forward. Already in this conference a variety of next generation lithographic technologies (NGLs) have been discussed, e.g., EUV and electron projection lithography, together with EB writing and x-ray printing. Some of them are also candidates chosen in the roadmap ITRS which appeared in the latter half of the first decade of this conference. Because the individual topics will be continuously discussed in this conference hereafter, I would like to make some comments below from a slightly different point of view.

## collaborated with DENSO ① Si Substrate 2 D-RIE ③ >1050℃ wet oxidation with Thick SiO2 -25 Output Power [dBm] -30 V<sub>DD</sub>= 2.0 V -35 25% power reduction Device formation 40 without Thick SiO<sub>2</sub> Inductor<sup>Transistor</sup> 3.0 4.0

Power Dissipation [mW

**MEMS** enhanced RF Circuits

Fig.3. A gigahertz CMOS RF Circuit utilizing MEMS process<sup>1,2</sup>

Hoh Fujishimja Lab

Passives are fabricated on thick oxide.

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One of the newly emerging field of lithographic applications is microelectromechanics (MEMS). Although this does not demand ultimately fine dimensions as the VLSI roadmap urges us, it needs to realize versatile types of three-dimensional structures with the cooperation of lithography and process technologies, e.g., engraving deep in the substrate or machining from the backside of the wafer. MEMS itself will not create a big market as VLSI did, but it will be one of the principal, off-roadmap applications of lithographic technologies and will in turn stimulate VLSI technologies in the next decade.

As an example of MEMS technique reversely imported by VLSI technology,  $30 \,\mu$  m-thick  $SiO_2$  was selectively formed in silicon substrate<sup>1</sup> as is shown in Fig.3. First, a series of  $30 \,\mu$  m-deep parallel trenches were engraved by RIE with the width and spacing of  $1 \,\mu$  m each. Then by oxidizing with wet  $O_2$ ,  $1 \,\mu$  m-thick silicon fins were entirely changed to  $SiO_2$  and they swelled to fill the trench-gap. Thus an almost uniform  $SiO_2$  block with the depth of  $30 \,\mu$  m was embedded locally in silicon substrate. By placing a spiral inductor on this  $SiO_2$  bed, a 1.5GHz CMOS RF circuit for ubiquitous communication was realized<sup>2</sup> with its power consumption reduced by 25% thanks to the suppression of parasitic capacitance and inductive current in the substrate. Another example of micro-mechanics applied to lithography technology is the dynamical correction of the distortion of the x-ray membrane mask by locally heating it with the light pattern<sup>3</sup>. Although a little bit sophisticated, this may shed light to the problem of stabilization of the x-ray mask.

Above are just examples. These and other novel applications are expected to stimulate lithography and related mask technologies through the next decade.

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