SIGEM, Low-temperature deposition of Poly-SiGe MEMs structures on standard CMOS circuits

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ABSTRACT

Fabrication of surface-micromachined structures by a post-processing module above standard IC circuits is an efficient way to produce monolithic microsystems, allowing nearly independent optimization of the circuitry and the MEMS process. However, until now the high-temperature steps needed for deposition of poly-Si have limited its application. SiGeM explores the possibilities offered by the low-temperature (450ºC) deposition and structuring of poly-SiGe layers, which is compatible with the temperature budget of fully-processed standard IC wafers.

In the SiGeM project several low-temperature deposition methods (CVD, PECVD, LPCVD) were developed, and were evaluated with respect to growth rate and material quality. The interconnection technology to the underlying CMOS circuitry was also developed. The capabilities of this new integration technology will be demonstrated in a monolithic high-performance rate-of-turn sensor, currently considered the most demanding MEMs application in terms of material properties of the structural layer (thickness > 10μm, stress gradient < 0.3MPa/μm) and signal processing circuitry (capacitance resolution in the aF range, SNR > 110 dB). System partitioning will combine analog and DSP circuit techniques to maximize resolution and stability. Parasitic electrical coupling within different parts of the system has been analyzed, and countermeasures to reduce it have been incorporated in the design.

The feasibility of the approach has already been proved by preliminary characterization of working prototypes containing released microstructures deposited on top of preamplifier circuits built on a 0.35μm, 5-metal, 2-poly, standard CMOS process from Philips Semiconductors. Resonance frequencies are in good agreement with predictions, and quality factors above 8000 have been obtained at pressures of 0.8 mTorr. Measured SNR confirms the capability to achieve a resolution of 0.015º/s over a bandwidth of 50 Hz.

Keywords: Poly-SiGe deposition, monolithic MEMs, surface micromachining, inertial capacitive microsensors.

1. INTRODUCTION

This paper reports on the work carried out during the first two and half years of the SIGEM project. The project, funded by the Commission of the European Union in its V Framework Program, aims to demonstrate the applicability of low-temperature deposition of Poly-SiGe, to be used as structural layer for monolithic micromachined sensors, as a post-processing step for industry standard CMOS wafers. If proven successful, this approach may become the dominant surface micromachining technique because it allows an almost perfect decoupling for the optimization of circuit and sensor technologies, currently provided only by two-chip implementations, while at the same time achieving the lower cost and parasitics reduction possible with a monolithic solution.

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2. PROCESSING OF THE MEMS MODULE

Poly-SiGe offers the advantage of a low deposition temperature, thus opening the possibility of building micromechanical structures on top of standard CMOS circuitry. However, there is a compromise between the temperature budget allowed by the CMOS technology, basically limited by the stability of the Al interconnect layers, and the deposition rate and mechanical quality of the structural layer. The developments made during the project have established that deposition temperatures of 450°C should not be a problem for Al wiring if it the deposition of each Al layer is followed by an adequate thermal conditioning. This is in line with the standard CMOS processing done by Philips.

The use of tungsten interconnects in all metal layers should allow for a higher poly-SiGe deposition temperature, but at the cost of deviating from industry standard CMOS processes, and creating an additional problem related to the bonding of the chip using standard procedures. This solution, although explored in the course of the project, was abandoned in favor of standard Al wiring.

Three different deposition methods have been followed to explore the possibility to have a structural layer complying with the requirements in terms of deposition rate, thickness, residual stress, stress gradient, and electrical conductivity (Table 1). The first method is LPCVD deposition in an ASM A400 batch furnace; the second is based on a single wafer process carried out in an ASM polygon module, using either APCVD or RPCVD, while the third path has explored the possibilities offered by PECVD. Most promising results have been obtained by a multilayered structure deposited using a combination of CVD and PECVD technique.

2.1. Development of the poly-SiGe Deposition Technology

The poly-SiGe structural layer should be at least 10 µm thick for increased sensitivity and to avoid excitation of out-of-plane bending modes for the gyroscope. Because of the low deposition rate of the LPCVD technique at 450 °C [1], a very long deposition time and hence a very high thermal budget is required to deposit this thick layer. On the other hand, the use of PECVD at 450 °C results in layers with a very high resistivity and compressive stress indicating that the films are probably amorphous. Thus, the poly-SiGe structural layer is deposited by using an advanced multilayer technology. This process aims at combining the best features of Plasma Enhanced Chemical Vapor Deposition (PECVD) and Chemical Vapor Deposition (without plasma), namely a high deposition rate and a low temperature crystallization, respectively. Initially a very brief PECVD layer is deposited (~94 nm) to avoid the large incubation time for the growth of SiGe on SiO_2, as normally seen in thermal CVD processes. This layer is amorphous and acts as a seed layer for the CVD layer on the top. The CVD layer serves as a crystallization seedlayer for the PECVD layer,

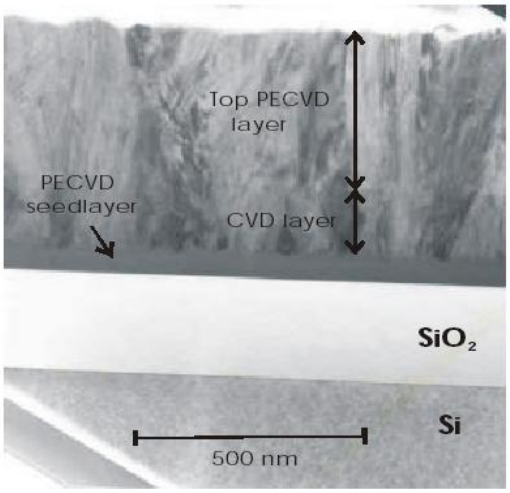
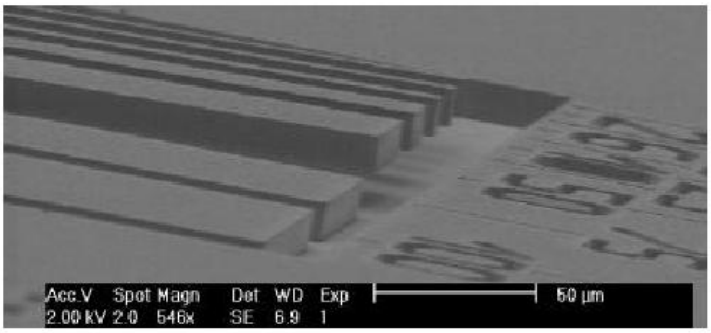


Figure 1 Cross-section TEM for a 1µm thick $Si_{35}Ge_{65}$ multilayer



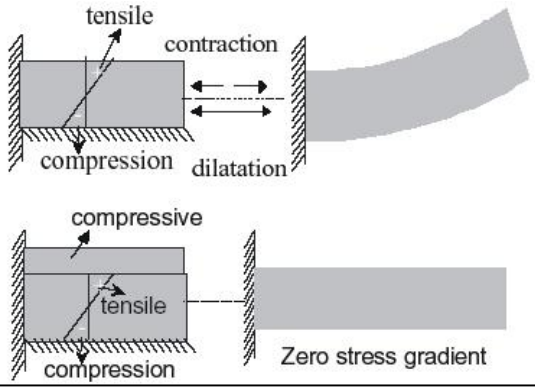


Figure 2. Strain gradient control by depositing a compressive top layer

thus making it possible to obtain a polycrystalline film at low temperatures (450°C) (Figure 1).

With this technique, high quality films are obtained at low temperature ($\leq$ 450 °C) with very high deposition rates (~100nm/min). The stress gradient in the layer is very critical to the performance of the gyroscope. The stress gradient in the layer can be fine-tuned by depositing layer of opposing stress behaviour on the top (Figure 2). A low resistivity of 0.9 mΩ·cm, a tensile stress of 57 MPa and a very low strain gradient of 1.2×10^{-5} μm^{-1} have been achieved so far [2].

An STS RIE-ICP etcher is employed for the dry etch of poly-SiGe. Alternating etch and passivation steps and adjusting the time for both gives very straight sidewall profiles with a smooth surface (Figure 2).

CMOS-integration also requires a low-resistance ohmic contact between the poly-SiGe structural layer and the top metal. The SiGe-Al contacts (Figure 3) of the integration wafer show an ohmic behavior (Figure 4) with a contact resistivity between 6×10^{-6} - 9×10^{-5} $\Omega\cdot cm^2$.

2.2. Overview of the MEMS module

The processing of the MEMS structures is done on top of 8" Al-based 0.35μm CMOS wafers from Philips with five metal levels and standard passivation. First an etch stop layer is deposited. Next bondpad holes are etched in the etch stop layer (figure 5, top-left). Sacrificial layer deposition and chemical mechanical polishing is carried out to planarize the surface (figure 6). Contact holes are opened by etching through the complete dielectric stack on top of metal 5. Poly-SiGe is then deposited to form the structural layer for the MEMS. Poly-SiGe is patterned using dry etching and finally the sacrificial layer is etched to release the MEMS structures (figure 5, top right).

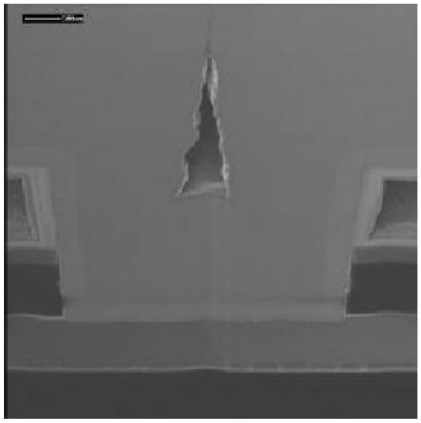


Figure 3. Filling of SiGe in the 28×4 μm^2 contact hole

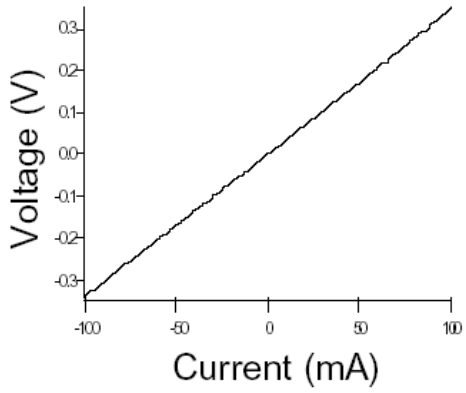


Figure 4. Ohmic contact

The sacrificial release is done using wet processing. Different solutions (BHF/Glycerol and HF/H_2O with different HF concentrations) were investigated to effectively etch the oxide and release the required structures without attacking the metal pads and underlying CMOS. BHF/glycerol is selective towards Al, but causes formation of residues that are difficult to get rid of. For the HF/H_2O solutions, it was observed that the selectivity in etch rate towards Al is not high, but it increases with increasing HF concentration. Hence, it was decided to use 49% HF followed by an IPA rinse to remove the sacrificial oxide. The step is time-critical in order to avoid attack of the Al bonding pads, but the required underetch time for the gyroscopes is short enough to obtain good results. CO_2 super-critical drying is used to eliminate stiction.

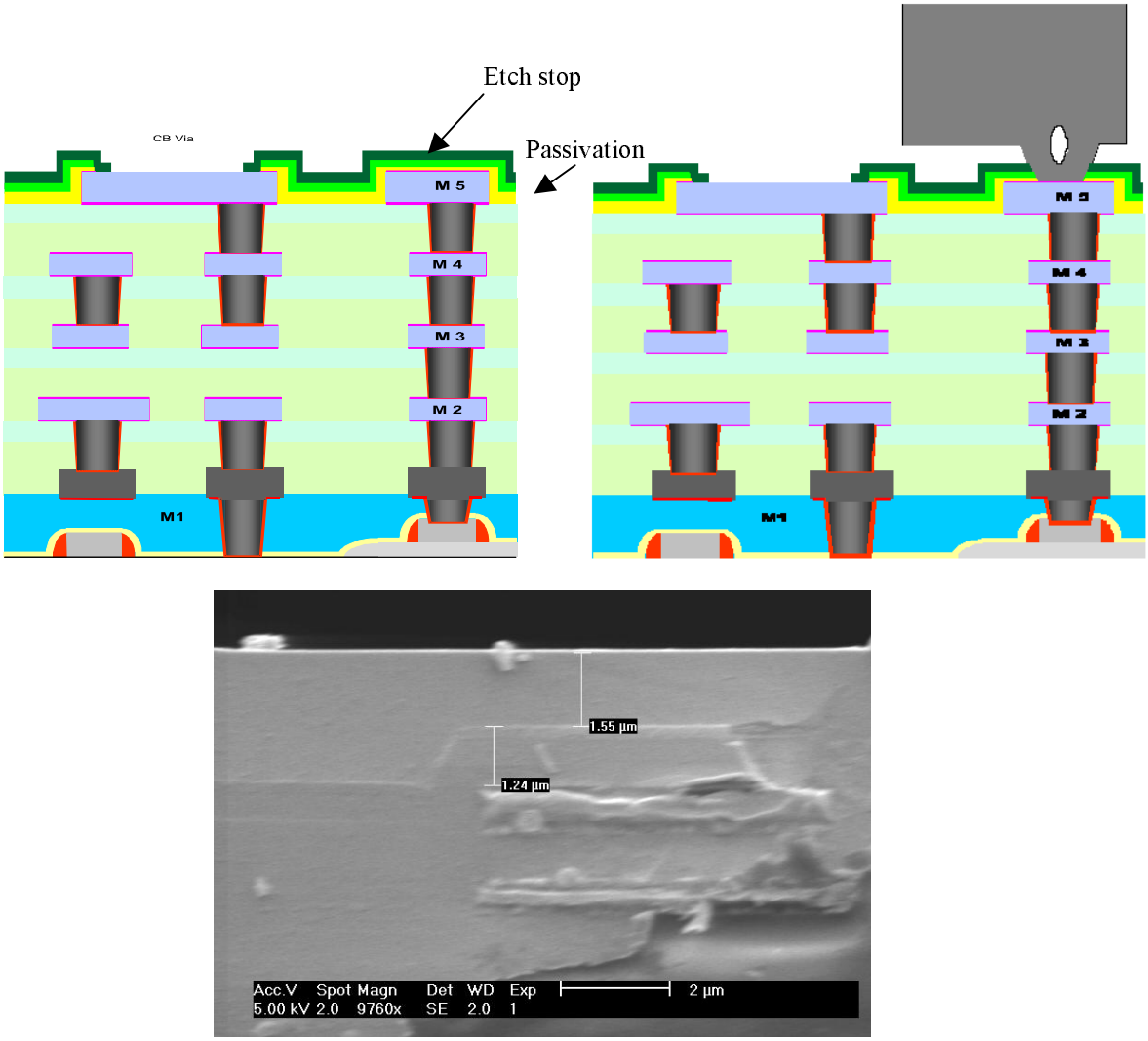


Figure 5 Backend Integration of Poly-SiGe MEMS over CMOS

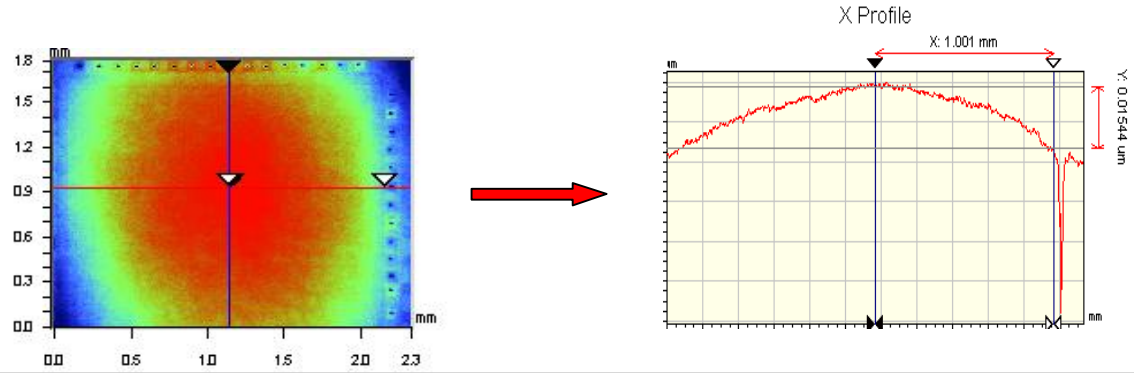


Figure 6 Results of CMP of the sacrificial oxide layer deposited on standard CMOS wafers having ~ 1µm topography. The remaining topography after CMP is only 10 – 15 nm over a mm-size chip area excluding the probed bondpads.

3. DEMONSTRATOR APPLICATION

The validation of the Poly-SiGe technology is made by its application in a real microsensor example. The application chosen has been a high-performance rate-of-turn (RoT) sensor, which currently constitutes one of the most demanding in terms of mechanical quality of the structural material and performance of the signal processing circuits. The system is planned as a demonstrator for a next generation of RoT sensor for automotive applications like car navigation and vehicle dynamics control (VDC). The basic requirements are a resolution of 0.015°/s in a 50 Hz bandwidth, and output drift of less than 0.5°/s over a temperature range of –40°C to +120°C. Mechanical resonant frequencies are in the 15-20 kHz range. The thickness of the structural poly-SiGe must be at least 10 μm, with stress gradient of less than 0.3 MPa/μm.

The system and structural layer specifications are given in Table 1 and 2.

Table 1. System Specifications

Parameter	Value
Range	± 100°/s
Noise (rms)	< 0.015 °/s
Measurement bandwidth	50 Hz
Offset-Drift	< ± 0.5°/s
Overload	± 1000°/s
Nonlinearity	< 0.2 %

Table 2. Structural Layer Specification

Parameter	Value
Thickness	> 10 μm
Deposition rate	> 10 nm/min (batch) > 150 nm/min (single wafer)
Stress gradient	-0.1 MPa/μm < SG < 0.3 MPa/μm
Residual stress	> -20 MPa (compressive) < 50 MPa (tensile)
Sheet resistivity	< 8 Ohm/square

3.1. Sensor geometry

The sensor element is based on a classical resonant structure with detection of the rate of turn based on the acceleration produced by the Coriolis force on a linearly vibrating structure. Capacitive combs are used for electrostatic drive and capacitive detection, including the establishment of the primary vibration mode, the detection of movements in the structure and the application of different test and compensation forces. Figure 7 presents a simplified diagram of the sensor geometry and the direction of movement of the different structural frames. A double-wing sensor is composed of two identical sections, each of them containing three different rectangular frames. Interdigitated linear combs placed in the two sides of the outer (drive) frame generate the electrostatic forces required to maintain the main vibration mode; this frame can only move in the X (horizontal) direction. The inner (detection) frame is constrained to move along the Y-axis. It contains parallel electrodes which form differential capacitive pairs; most of them are used for detection of the movement produced by the Coriolis force, and the rest are used for application of test and compensation forces. There is a third (intermediate) frame that is free to move in the X and Y directions. When an input RoT is present, the outer and intermediate frames vibrating at full amplitude along the X-axis contribute to the generation of a Coriolis force in the Y direction. This force is transmitted through the intermediate frame to the inner frame producing a displacement along the Y-axis which can be sensed by the detection electrodes. The two sections of the sensor are driven in counterphase. An external acceleration will then appear as common-mode signal for the two halves, while the Coriolis forces act as a differential signal. Subtracting the outputs of the detection electrodes will give only the contribution of the differential Coriolis movements and cancel the common-mode acceleration and noise components.

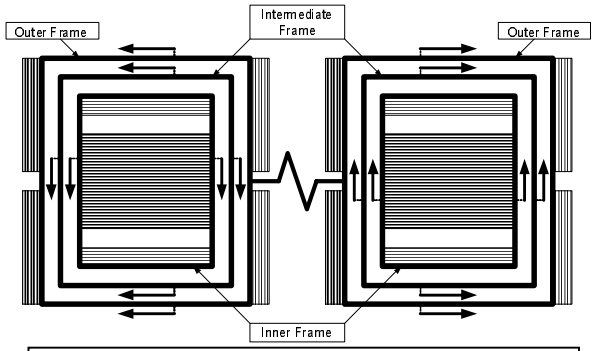


Figure 7. Simplified structure geometry

The drive frame operates at large vibration amplitude (10μm) and when an input rate-of-turn is present, it produces a Coriolis force that is transmitted to the detection frame. The spring arrangement decouples the drive and detection

frames, to reduce the effect of position dependent quadrature forces, induced by imperfections in the elastic supports of the drive frames.

Differential capacitor combs detect the movement generated by the Coriolis force. To maximize sensitivity, the resonant frequency of the detection frame is electrostatically matched to the resonant frequency of the drive mode. Partial compensation of the parasitic quadrature movement in the detection combs is achieved by sets of dedicated electrodes producing a force proportional to the displacement of the drive frame. A DC voltage applied between the anchored quadrature-compensation electrodes and the moving frame adjusts the magnitude of the force.

3.2. System partition

The high-performance system requirements, particularly in what concerns output stability, advises the use of a mixed-signal approach, with the bulk of the signal processing made using digital techniques and analog functions limited to the front-end amplifiers, drivers, and A/D or D/A converters. A basic block diagram of the full-system is shown in figure 8. Because of the flexibility needed for a new technology and system concepts, the digital signal processing functions are implemented in an external FPGA (Spartan-2E from Xilinx). This approach permits fine tuning of processing parameters and even modifications to the algorithms used in the various control loops used in the system. However, to test the capability of the analog blocks to perform adequately in a mixed-signal environment, as will be the case in an actual application, a relatively large digital block, consisting of the decimation filter and signal level detector for the sense signal has been included on-chip. This whole block can be enabled or disabled to verify the effect of its activity on noise performance.

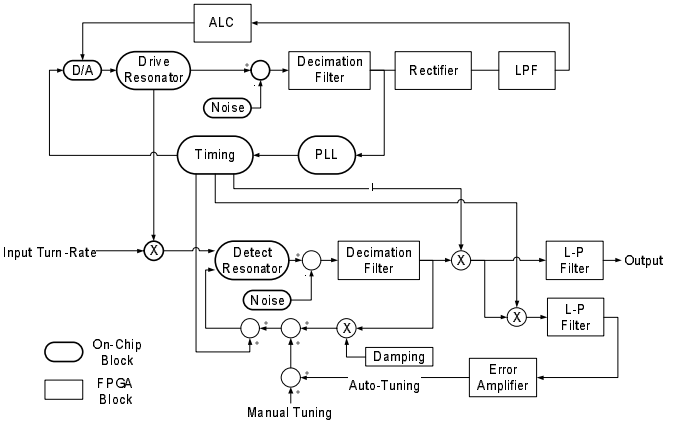


Figure 8. Block diagram of demonstrator system

There are two main subsystems. The first (drive-loop) maintains the main vibration at constant amplitude at the mechanical resonance frequency of the drive mode. The feedback loop generates a driving voltage with the phase needed to maintain the oscillation. Synchronous demodulation and low-pass filtering detect the amplitude of the movement. A fully-digital Automatic Level Controller (ALC) generates a high frequency, second-order noise-shaped, 4-bit word to control a variable attenuator that fixes the amplitude of the electrostatic feedback force applied to the resonator. The output of the resonator is also used as reference input for a PLL that generates the timing signals required for system operation. Because the digital clock supplying the DSP is a fixed multiple of the resonator frequency, the filter characteristic remains unchanged against sensor-to-sensor variations in the mechanical resonance.

The second subsystem deals with the detection of the movement induced by the Coriolis force. When the system turns around its sensitive axis, the drive frame-set produces a Coriolis force proportional to the product of the speed of the drive movement, and to the input RoT. Thus the detection mode output is basically an Amplitude-Modulated Suppressed-Carrier (AM-SC) signal, with its carrier in phase with the drive mode speed and with an amplitude proportional to the input RoT. Because the amplitude of the drive mode is maintained constant by the ALC, the AM-SC signal can be demodulated synchronously to obtain a voltage proportional to the input RoT. Other functions included in the detection subsystem are the electronic adjustment of the damping factor by application of an electrostatic force proportional to the linear speed of the detection combs; the adjustment of the detection mode resonant frequency using the negative spring constant resulting from application of a DC voltage to the test electrodes; the generation of a test force to verify correct sensor operation, and finally the application of a spread-spectrum low-power excitation for on-line measurement of the mismatch in resonant frequency between the drive and detection modes, eventually leading to automatic frequency matching.

3.3. Drive loop

The movement of the drive frame is sensed from the current generated in the sensing combs, which are biased with a constant voltage difference. The movement of the frame induces a current proportional to its linear speed. That current

goes into a two-stage continuous-time charge amplifier. The differential signal at the amplifier output is an AC signal with amplitude proportional to the displacement of the drive frame.

The output of the amplifier section is fed to a second-order S-D modulator, as first step for the A/D conversion of the signal. The output of the modulator is a one-bit stream that is passed through a digital low-pass filter to reject the high-frequency quantization noise. Because the filtered signal has to contain accurate information about the phase of the drive movement, all filtering is done at the highest possible frequency, which is the operating frequency of the S-D modulator. The filtered signal is used as reference clock for an on-chip PLL that generates a number of timing signals synchronized with the drive movement.

3.4. Detection of Coriolis force

The Coriolis force excites the movement of the detection mode resonator, that will be electrostatically tuned to have the same resonance frequency as the drive mode. The input RoT produces a movement along the Y-axis as an amplitude modulation with its carrier at the same frequency as the main drive mode movement. The output signal, proportional to the rotational velocity is obtained by synchronous amplitude demodulation, followed by low-pass filtering.

In the ideal case, when only the Coriolis force is present, the phase noise represented by the phase difference between the demodulation clock and the Coriolis induced carrier will appear attenuated at the output. However, if a parasitic quadrature movement is superposed along the detection axis, it will have a large effect in the output noise, because the phase noise affects the demodulated output close to the peak of the quadrature signal. Thus, in that case, the combination of quadrature amplitude and phase noise, rather than amplification noise, may easily become the main factor determining the achievable resolution.

3.5. On-Chip Electronic Blocks

Front-End Amplifiers

Two different approaches have been tried for the low-noise capacitance-to-voltage converter needed to sense the movement of the structure (figure 9). The first one is a classical approach using S-C, correlated double sampling (CDS) techniques, while the second is based on a variation of the continuous-time reset technique proposed in [3], using as feedback resistor for the C/V converter a very low-transconductance MOS transistor, operating in the sub-threshold triode region, and capable to provide resistances larger than 1 TΩ.

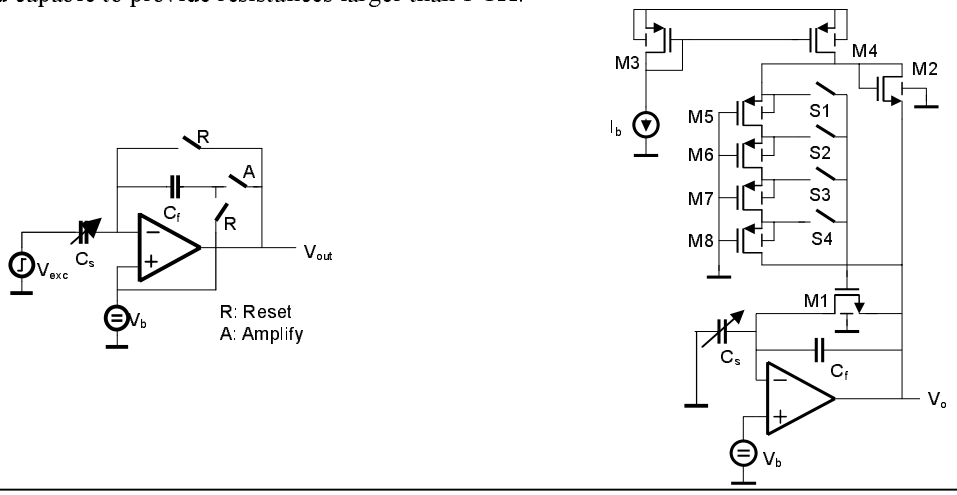


Figure 9. Alternative charge amplifier architectures. left: classic S-C, CDS amplifier; right: continuous-time reset amplifier

In the S-C architecture, the output noise is dominated by undersampling (folding) of amplifier thermal noise and by feedback capacitor *kT/C* noise. Best output SNR is obtained reducing the feedback capacitance and increasing the sampling frequency. At high sampling frequencies the SNR tends asymptotically to a limit determined basically by the amplifier noise.

With the continuous-time reset approach the main contribution to output noise comes from flicker noise in the amplifier and in the MOS feedback resistor. The SNR is improved if the area of the input stage transistor is increased, but beyond

a certain value, the extra parasitic capacitance starts to degrade it. The value of the feedback capacitance has only a secondary effect in SNR for this type of amplifier.

While the first prototype was implemented using S-C amplifiers, the final device uses the continuous-time approach, as experimental results have demonstrated that it can give a better SNR.

Crosstalk Effect on Output Stability

The main disadvantage of the use of the continuous-time amplifiers operating in baseband is the capacitive croostalk from the driving electrodes to the high impedance nodes at the input of the sense and detect amplifiers (fig. 10). The driving electrodes carry a time-varying voltage that through parasitic capacitive coupling induces a crosstalk current (I_p) in the sensing nodes. The main harmonic of the parasitic current is in quadrature with the sense current component, and introduces a phase error in the detected signal with respect to the actual movement in the structure. That error translates in a level shift of the detected rate output signal. If the amplitude of the drive voltage were constant in all operating conditions, this effect could be easily compensated, as it would appear as a constant output offset. However, the drive amplitude has to change to adapt to environmetal variations, like for example changes in the Q factor due to temperature or aging. Calculations show that the crosstalk capacitance has to be below 100 aF to keep output drift below 1% of FSR in the presence of a quadrature movement with amplitude 10 times larger that the FSR of the RoT signal.

Electrostatic analysis of the capacitive coupling in the different electrode combs has been performed to estimate the amount of crosstalk coupling. QuickField ™, a 2-D FEA CAD tool [10] has been used in the analysis. The simulation results have been useful to modify the layout of the structure, to benefit as much as possible from the electrostatic shielding provided by interposed electrodes connected to low impedance DC voltages, and from the crosstalk cancellation resulting from electrical balance and geometric symmetry. The availability of five metal layers has also proved valuable in shielding the interconnection lines carrying the driving voltages, while at the same time allowing to have the electronics underneath the gyroscope structure.

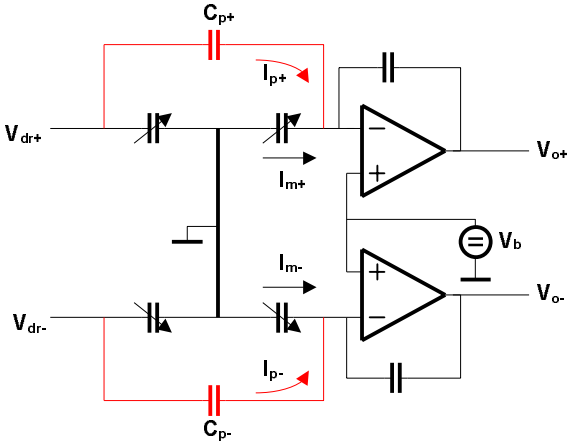


Figure 10. Capacitive crosstalk current (I_p) from driving electrodes

Programmable-Gain Differential Amplifiers

A fully-differential amplification stage follows the single-ended C/V amplifiers. As with the front-end amplifiers, in the first evaluation prototype the differential amplification stage has been implemented with a classical S-C circuit, while the final device uses the continuous-time reset solution.

The differential amplifiers have programmable gain with seven steps between –9 dB and +9 dB to adjust their output amplitude to the optimum value for the input range of the S-D modulators that follow them. Because a change in amplifier closed-loop gain produces a change in its bandwidth, dummy load capacitors placed at the amplifier output are simultaneously changed to keep the resultant bandwidth approximately constant and minimize the changes in phase of the output signal, which otherwise would affect the DC level (drift) at the output of the synchronous demodulator when a parasitic quadrature component is present.

S-D Modulator

The analog-to-digital conversion of the sense and detect output signals are performed by an on-chip second-order S-D modulator, followed by a decimation filter implemented in the external FPGA. With the oversampling rate available (256 samples per cycle of the resonator signal), such a modulator is the simplest S-D architecture able to provide the SNR required by the application.

The signal-to-noise ratio achievable when the noise is integrated in the Nyquist band is:

$$SNR = 50\log(OSR) + 20\log\left(\frac{A}{\Delta}\right) + 10\log\left(\frac{60}{2\pi^4}\right)$$

with A being the signal amplitude, Δ the quantization step and OSR the oversampling ratio.

In our case, the noise has to be integrated only over the output measurement bandwidth (Δf).

$$SNR' = 50\log OSR + 20\log\left(\frac{A}{\Delta}\right) + 10\log\left(\frac{60}{2\pi^4}\right) - 10\log 5 + 10\log\left(\frac{f_O}{\Delta f}\right)$$

Substituting the values expected in our system for conversion of the detect output, the theoretically achievable Nyquist-band SNR is 92,0 dB, and SNR' is 106 dB, a value 12,6 dB above the required specification. Thus a second order modulator offers sufficient margin to accommodate implementation errors. The target values used in the analysis leave margin for a parasitic quadrature component with an amplitude up to ten times larger than the output FSR.

The design of the modulator was made using ASIDES, a proprietary CAD tool for high-level design of switched capacitance S-D modulators, developed by researchers at IMSE [6,7]. The tool allows a fast optimization of modulator performance, including second-order effects, like amplifier and kT/C noise, amplifier gain error, distorsions and incomplete charge settling. Figure 17 shows simulated results from ASIDES, compared to values measured in the actual implementation of the S-D modulator, processed as part of the final integration run.

Phase-Locked Loop/VCO

The system incorporates an on-chip PLL, locked to the output proportional to the movement of the drive frame. The PLL is an integral part of the control loop of the drive-mode oscillator. It provides the phase information required to set the main vibration mode. It is also used as reference to generate the timing signals necessary for operation of the S-D modulators and the DSP logic in the external FPGA.

The core of the PLL is a differential low-noise voltage-controlled CMOS ring oscillator [9]. The frequency of the VCO is primarily determined by the transconductance of its input stage and its output load capacitance. Frequency tuning is done by adjustment of the input pair bias current to the value needed to give the required transconductance value. The differential control voltage is generated by a Phase-Frequency detector followed by a charge-pump circuit and a passive second-order compensation filter.

Amplifier Bandwidth Control

The main source for output drift comes from changes in the phase difference between the detection mode carrier signal, and the oscillator used to demodulate it, which is derived from the movement of the main drive mode. In baseband operation, that phase shift is modified by changes in the frequency response of the front-end amplifiers. With the OTA amplifiers used in the design (folded-cascode) the bandwidth is determined basically by the input stage transconductance and the capacitive load at its output.

If the same type of MOS transistor is used in the input stages of the OTA amplifiers and in the VCO ring oscillator, then it is possible to implement a mechanism for open-loop control of the amplifier bandwidth, if the amplifier bias current is obtained by scaling the bias current of the ring oscillator. Because the VCO is locked to the drive mode mechanical resonance frequency which is practically independent of operating conditions, its bias current will be at a value that maintains its input transconductance constant. Then the input transconductance of the charge amplifiers will also remain constant and its bandwidth will not be modified by operating conditions.

Experimental results obtained with the first prototype chip indicate that with an amplifier bandwidth ten times higher than the mechanical resonance frequency, if its bias current is a scaled copy of the VCO bias current, the phase shift introduced by the amplifier at the resonance frequency will remain constant versus changes in temperature within $\pm 0.1^{o}$.

High-Voltage D/A Converter

The on-chip generation of the drive voltage for establishment and amplitude control of the main mode vibration is made by an oversampled D/A converter. The converter (figure 11) is composed of two parts: a variable 4-bit attenuator, driven by an oversampled control word, that adjusts the driving voltage amplitude, and a shaper to reduce the harmonic contents of the driving voltage.

The attenuator is driven from the digital output of the PID Automatic Level Controller implemented in the external FPGA. This is a low-frequency signal that is passed through a second order S-D modulator. The control word is updated 16 times per cycle of the drive voltage. The noise shaping given by this oversampling frequency combined with the low-

pass filtering of the resonator response to drive amplitude changes provided by the high mechanical Q of the drive mode - with an effective worst-case bandwith in the order of 20 Hz – results in a simple and robust D/A converter with a theoretical resolution of more than 30 bits.

The shaper is made from a resistive attenuator chain followed by an analog multiplexer which applies to the driving combs one of the voltage levels in the attenuator. The multiplexer is driven by a timing signal derived from the on-chip PLL, and locked to the mechanical vibration. The design uses nine voltage levels, switched at a frequency giving 16 samples per cycle of the drive voltage. The values of the resistors in the ladder can be adjusted to give any desired shape to the generated voltage. In our case, because the structure in the final device is driven from only one side of the inertial frames the voltage follows the shape of the square root of a sinusoid, resulting in a sinusoidal electrostatic force applied to the drive combs.

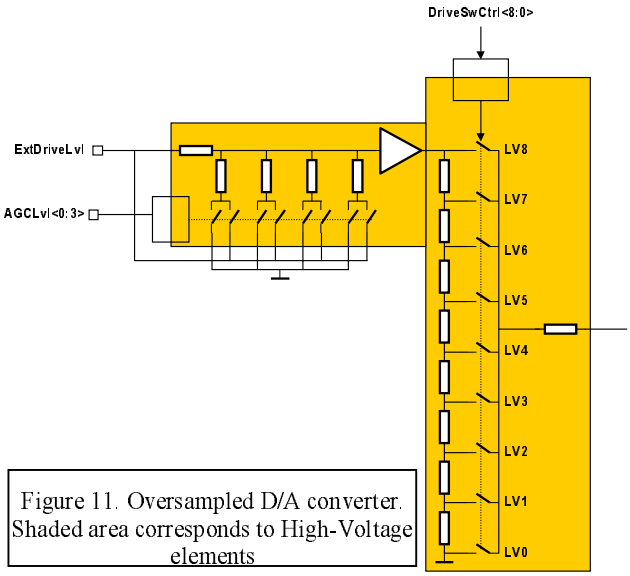


Figure 11. Oversampled D/A converter. Shaded area corresponds to High-Voltage elements

3.6. Off-Chip Electronic Blocks

The use of an new technology, not yet fully characterised, and of system concepts and algorithms not tested before, leaves a degree of uncertainty in the design of the system. To have sufficient flexibility to accommodate functional changes, the digital signal processing functions will be implemented in an external FPGA. In this way, algorithms and system parameters can be easily modified if needed. All the system, has been extensively simulated using MATLAB's SIMULINK, and the blocks corresponding to the DSP functions can be mapped into VHDL code with the System Generator tool. The VHDL code so generated can be integrated with the rest of the functional VHDL code, and mapped into Xilinx FPGA hardware using the ISE tool. This method provides a fast way for verification and implementation of modifications to the DSP algorithms.

The functions included in the FPGA are:

1) decimation filters for the outputs of the two S-D modulators; this filtering also performs the phase shift required to have the proper phase for the voltage generating the electrostatic force feedback in the drive-mode resonator loop.
2) Rectifier, low-pass filter and PID controller for the Automatic Level Control loop that maintains a stable vibration amplitude of the drive mode.
3) Synchronous demodulation and low-pass filtering of the Coriolis movement, needed to extract the RoT output signal.
4) Electronic adjustment of damping in the Coriolis detection mode.
5) Detection and, if feasible, automatic correction of resonant frequency mismatch.

4. EXPERIMENTAL RESULTS

An early decision adopted by the project partners was to try to obtain as soon as possible an intermediate demonstrator that would put to test the complete range of processing steps required to manufacture a monolithic gyroscope. Therefore a simple chip containing a micromechanical structure linked to an electronic circuit integrated in the substrate was already included in a first integration run. Initial project plans called for separate characterization of the electronic blocks and poly-SiGe micromechanical structures. This solution would have provided quicker results but would have left hidden potential problems coming from the design and manufacturing flow and from the interface between the structure and the electronics. Although the decision introduced some delays in the project, it was considered worthwhile given the potential for reduction of manufacturing time needed for the final prototype, and minimization of risk in future runs by early detection of design and process flaws. What is more important, it was a useful practice run to streamline the

procedures needed for exchange and preparation of design and manufacturing information between partners cooperating from four different locations.

Apart from the specific runs needed for development of the poly-SiGe layer, during the project there have been two completely processed manufacturing runs, both including CMOS circuitry and surface micromachined structures. Both integration run also included a test chip for characterization of individual electronic blocks. The first integration run had several versions of simple monolithic sensors, based on existing non-optimized designs of double- and single-wing gyroscopes, together with the electronic circuitry needed to detect the movement of the structure along its two main axes. Target at this stage was not so much device performance as to prove that the ellaborated design and manufacturing sequence could produce working monolithic circuits, with released poly-SiGe structures built on top of a fully processed standard CMOS wafers.

The processing of the CMOS part of the final integration run has been completed, and experimental results are available for the electronics-only chip. Processing of the structural layer was being completed at the time of this writing.

4.1. Results from the First Integration Run

As mentioned above, the first demonstrator contained chips with double- and single-wing gyroscope plus amplification stages to detect the movement of the two modes of the gyroscope (drive and Coriolis). The internal circuitry was kept to a minimum to reduce the delay in project timing, but still tried to be representative of the one to be used in the final prototype. The amplification stages were realized using S-C CDS techniques, and incorporated two single-ended amplifiers for detection of movement in each of the two axis. Analog buffers were also added to reduce the output signal impedance to levels compatible with the external circuitry and instrumentation to be used in the characterization. A small on-chip digital block was implemented to generate the non-overlapping clock signals required for operation of the S-C amplifiers. The voltage to set the main drive movement was injected directly from outside the chip. A simplified block diagram of the circuitry included in the chip is shown in figure 13.

Figure 12. First run test board

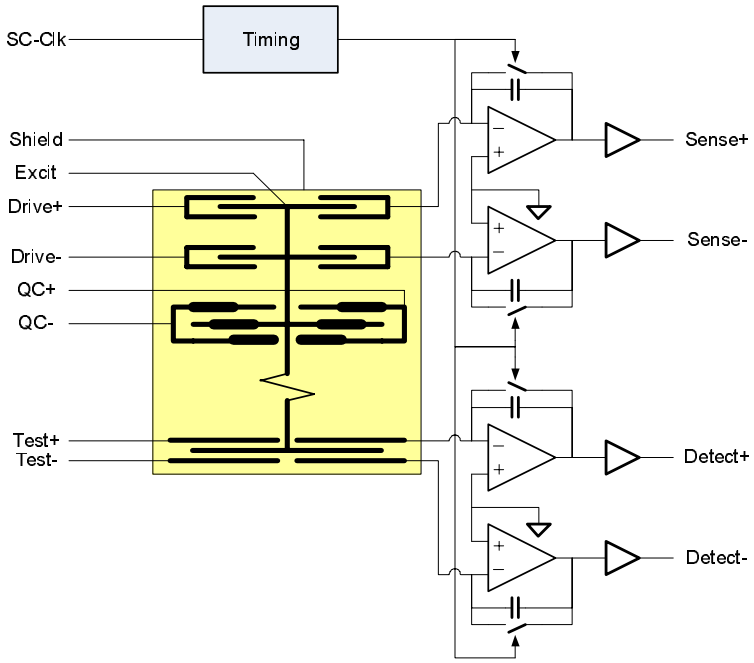


Figure 13. Block diagram of demonstrator system

The test chip was encapsulated at atmospheric pressure in a 44-pin metal-can package. The package cover was not welded to permit operation at reduced pressure by placing the device in a vacuum chamber. A test board (figure 12) was designed containing the auxiliary circuits needed to excite and sense the response of the two movement modes, and to demodulate and amplify the readout signal coming from the on-chip front-end amplifiers.

Measurements have been carried out both at atmospheric pressure and in vacuum. The sensitivity at ambient pressure is enough to determine the resonance frequency for both modes. Tests in vacuum (~ 1mTorr) provide a more accurate characterization and also give an assesment of the Q factor that can be achieved with Poly-SiGe. An example of the response in vacuum for the sense mode is shown in figure 14. The symmetry of the resonance peak proves that at full range drive amplitudes nonlinear effects are negligible. Measured Q at 1 mTorr is in the range of 8000-10000 for the sense mode, and 4000-6000 for the Coriolis detect mode.

Extrapolation of the results to the conditions expected in the final prototype confirms the feasibility of meeting the target resolution (0.015º/s)

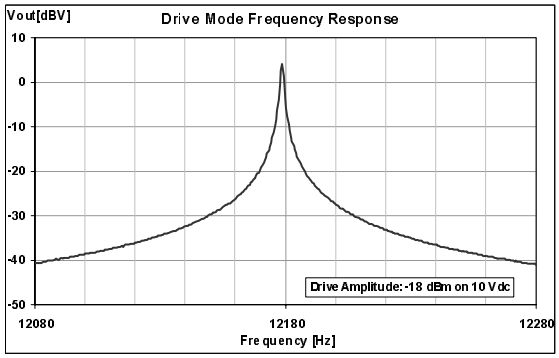
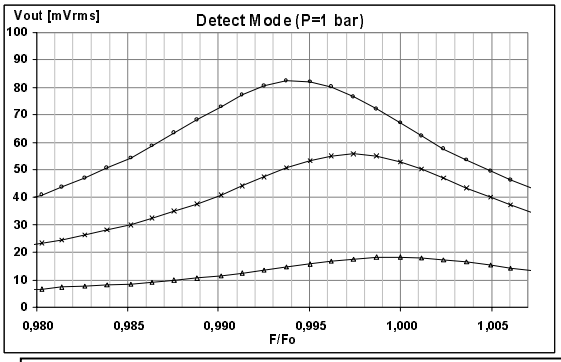


Figure 14. Frequency response measured in vacuum



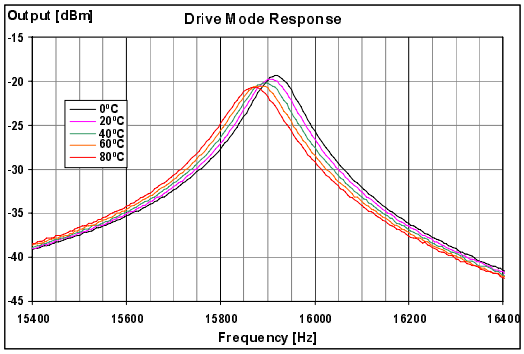


Figure 15. Left: Shift in resonance frequency of the detection-mode with change in DC level of driving voltage. Right: Change with temperature of drive-mode resonance frequency

The graphs in figure 15 are a demonstration of the characterization possible at atmospheric pressure. Figure 15-left shows the shift in the resonant frequency of the Coriolis detection mode when the DC voltage of the signal driving the test combs is modified. A larger DC component increases the net electrostatic force, seen as an increment in the resonance peak amplitude. At the same time, it increases the magnitude of the electrostatic negative spring constant, and the resonant frequency decreases. This effect will be used to achieve the matching of the resonance frequencies of the drive and Coriolis vibration modes. Figure 15-right gives the change in the open-loop frequency response of the drive mode when the temperature changes from 0ºC to 80ºC, the peak amplitude changes 1.4 dB, and the resonant frequency shows a temperature dependance of approximately 40 ppm/ºC.

4.2. Results from the Final Prototype Run

The second manufacturing run is aimed to the development of a demonstrator rate-of-turn sensor. The final chip, which incorporates nearly all analog blocks required for a fully operational sensor, is currently being manufactured. The digital processing is done off-chip in an FPGA. A chip for characterization of the individual analog blocks was also designed in this run. Results shown in this section correspond to this characterization chip, as the monolithic sensor is not yet ready at the time of this writing.

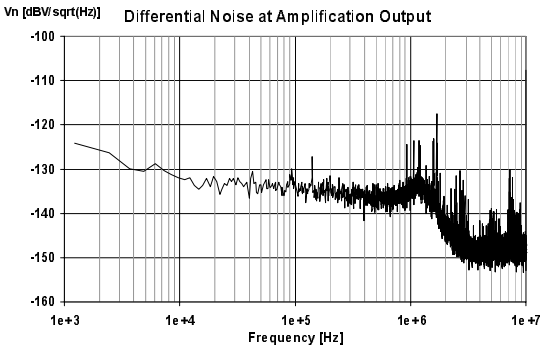


Figure 16. Noise at the output of the amplification chain.

The continuous-time amplifier noise performance is shown in figure xx which represents the differential noise at the output of the amplification chain, just at the input of the S-D modulator, where the expected signal level is approximately 0.5 V_{rms}. For that signal level, the spectral noise density in the proximities of the 20 kHz frequency region should be lower than –120 dB/sqrt(Hz) to have a SNR better than 94 dB over a 50 Hz bandwidth.

The performance of the continuous-time amplifier should then be more than sufficient to meet the resolution specification.

Note that the measurements have been made in a test chip containing all the blocks of the final demonstrator with the exception of the micromachined layer.

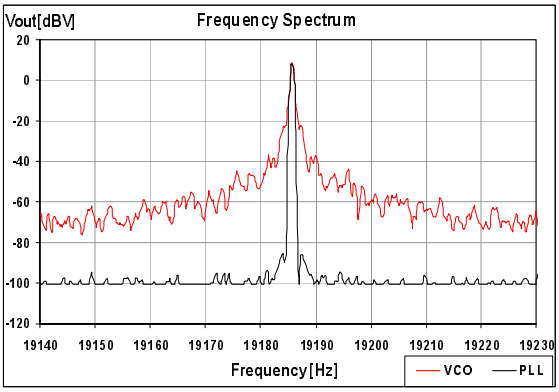


Figure 17. Frequency spectrum of free-running VCO and VCO locked to an external source

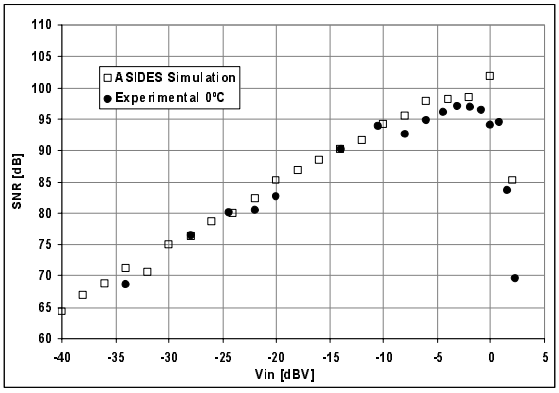


Figure 18. Simulated (ASIDES) and experimental SNR overload curves for Σ–Δ modulator

The performance of the PLL with respect to its ability to reduce phase noise between the resonator and the local VCO used for demodulation is depicted in figure 17 which shows the spectrum of the free-running VCO output compared to the VCO spectrum when the PLL locks it to an external stable frequency reference. The difference between the two curves (~40dB) is a measure of the excess gain in the control loop available for reduction of phase noise between the mechanical resonator and the VCO.

Figure 18 presents the overload characteristic of the Nyquist bandwidth SNR of the S-D modulator as a function of input amplitude for experimental results compared to the predictions generated by ASIDES high-level simulations. The agreement is very good and is typical of the quality of the results that can be obtained with ASIDES. The experimental curve at 0°C is shown as this was the one giving worst-case results.

5. CONCLUSIONS

The project has proved the feasibility of the fabrication of surface micromachined structures using a thick poly-SiGe layer.deposited on top of industry-standard fully processed CMOS wafers. The mechanical properties of the layer are close to the values needed for high-performance inertial sensors.

The performance of the on-chip signal processing circuitry has been demonstrated for stand-alone blocks. Full system validation is pending on the availabilty of the final prototype monolithic chips.

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