The Evolving Complexity of Patterning Materials

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ABSTRACT

People have enjoyed innovations which are made possible with the device scaling. The industry has been challenging to realize the Moore's Law. Resolution limit of ArF immersion scanner has already been larger than the device CD necessary now. Device structures have been getting more and more complicated to meet various technology requirements such as scaling, device speed, low power consumption and so on. Not only the scaling but also complication has to be overcome to realize those requirements. Scaling requirements, device structure, and new types of architectures for new generation device with the limited single exposure capability force us to keep using and exploring complicated multi-step patterning techniques or "tricks". Device design, elements, process, and consumable tricks and JSR's solution have been reviewed.

Keywords: Photoresist, Scaling, Hardmask, EUV, DSA, Slimming, Process trick

1. INTRODUCTION

Many things have been smaller, more convenient, and more functional in our life. People have enjoyed all of those innovations which are made possible greatly with the device scaling. Process scaling has never ended although it was predicted to come to end various times. The industry has been challenging to realize the Moore's Law [1]. Resolution limit of ArF immersion scanner (~40nm) has already been larger than the device CD necessary now [2]. Device structures have been getting more and more complicated to meet various technology requirements such as scaling, device speed, low power consumption and so on. Not only the scaling but also complication has to be overcome to realize those requirements. Device 3D structure and new types of device increase the complexity. 3D structure has to deal with its unique requirements for material and process as well as metrology. "Tricks" have been used to achieve the scaling in many ways like device design, elements, process, and consumable tricks.

2. TRICKS FOR THE SCALING

2.1 From the design side

The logic transistor went into the three dimensional structure from the two dimensional for 22nm. So-called Fin-FET or tri-gate transistor structure has been developed and it has already been in mass production [3]. DRAM and NAND memories have leaded the scaling. However, DRAM has already faced the density challenge. Even 3x nm device capacitor requires very high aspect ratio structure. Process to make 2x nm capacitor will be a real challenge and there may be a cell capacitance concern. NAND process scaling has already been close to 1x nm where the critical number of electrons is limited with a fundamental concern how to manage just tens of electrons. Hence, various three dimensional NAND architectures have been studied to extend the scaling. With such challenges for DRAM and NAND, new types of memories have been proposed and studied for improved scalability and reliability like PCRAM, MRAM, ReRAM, and Race track memory [4], [5].

2.2 From the elements side

A lot of new materials have been introduced to advanced device production beyond 90nm generation (or since 65nm generation) together with complicated and non traditional, sometimes very tricky, processes. A lot of new elements have been introduced to improve device performance. Ge was used to strain Si lattice in the source/drain region [3], [6]. High k materials like hafnium oxides were used for high-k metal gates and DRAM capacitor [3], [7]. Low-k dielectric materials and new tools for deposition have been used for Back End process [8], [9]. III-V group elements have been studied for new high mobility channel materials [3]. New memories explored new materials like magnetic substances for magnetic memories. Now nano technology including new forms of materials like carbon nanotube, nano wires and fullerene are studied for future technology [3].

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2.3 From the process side

Advanced patterning techniques such as O.A.I, O.P.C, S.M.O, immersion lithography, and double patterning have been used in production [3], [10]. Design for manufacturing (DFM) has been used for lithography process [11]. Device design is optimized for lithography process from the very beginning for better process window. More litho-friendly design has been taken for the circuit design with more single directional patterns for better process. Dummy patterns are added for better process window. Computer and simulation have been used to optimize the source shape and mask design to achieve very low k1 factor lithography. To use the calculated source shape effectively, advanced tool option like ASML's FlexRay is developed and applied [12], [13]. Even with the above techniques, physical limitation of single exposure forced us to explore various double patterning techniques. Now self aligned double patterning (SaDP) is very popular and proved to create small CD [14]. Advanced oxide deposition tools for accurate CD control have been introduced. One dimensional patterning with cut mask to create SRAM like features is now very popular [15], [16]. Litho-etch-litho-etch (LELE) double pattering is also studied and used as well.

2.4 Tricks from the consumable side

Due to the resolution limitation of single exposure, double patterning techniques are used in multi-steps. Hardmask (HM) is very essential in complicated multi-step process. In addition to traditionally existing hardmask materials like nitride, oxide, and carbon deposited film, new hardmask materials have been studied to strategically differentiate etch selectivity from existing materials. Various new chemicals associated with complicated processes are studied and used. The examples are clean chemicals, thermal resistant HM, high modulus HM, wet-cleanable HM, faster dry etch HM, and spin-on image reversal materials. New technology such as DSA could be used for production and hence new materials for such technology should be developed. 10nm or beyond device production would need more and more dedicated, tailor made, but preferably economical material for each step.

3. JSR TRICK MATERIALS

JSR has been extensively working on advanced materials development with customers and partners for necessary tricks to achieve device scaling. Among many tricks, several important trick materials are reviewed: Advanced EUV photoresist, slimming agent, shrink material, DSA material, Organic spin-on HM for EUV lithography, and spin-on metal HM.

3.1 Advanced EUV photoresist

EUV is still an encouraging candidate for the next generation lithography to enable smaller CD because of its simpler single exposure process. Extensive research has been done to develop this technology, especially the tools and materials. Resist is still one of the most important materials for the technology. Now the ASML's NXE3100 scanner is available for exposure as well as MET tool. JSR has collaborated with customers to develop photoresist materials and establish the high volume manufacturing process. We have developed various encouraging high resolution photoresists with reasonable photosensitivity and LWR. Example is shown in Figure 1. There are still many question marks with various issues. JSR will continue R&D for EUV lithography to contribute to the industry to make EUV lithography possible.

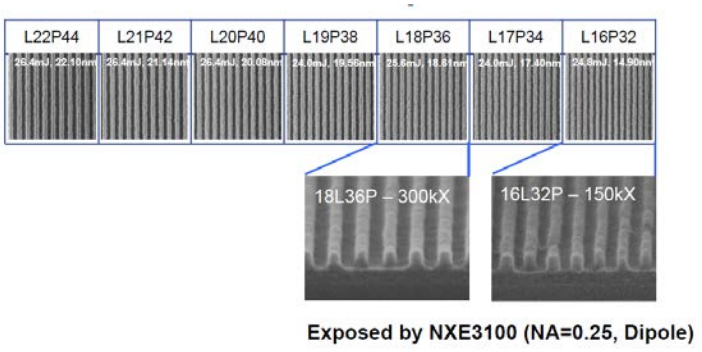

Figure 1. JSR's EUV photoresist performance.

3.2 Slimming agent

In the SaDP process, the litho patterns sometimes are necessary to slim down to be covered by oxide film. Dry etch trim is one way for CD slimming. However, all in the track slimming CD process with spin-on material is desirable from the through-put and cost points of view. JSR has researched and developed a track friendly spin-on solution with performance as shown in Figure 2. CD size can be slimmed down to desirable level while still maintaining the good process window.

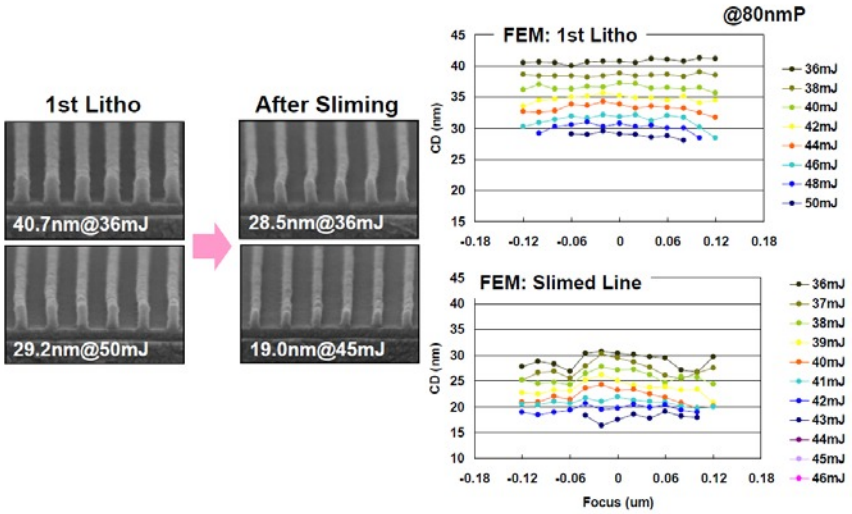

Figure 2. JSR Slimming material performance.

3.3 Shrink material

For double patterning like LELE process, often small trench patterns are necessary. However, due to the scanner resolution limitation of the single exposure, the litho trench patterns should be treated to smaller size. Chemical shrink is an economical, track friendly solution. JSR has studied and developed shrink materials as shown in Figure 3.

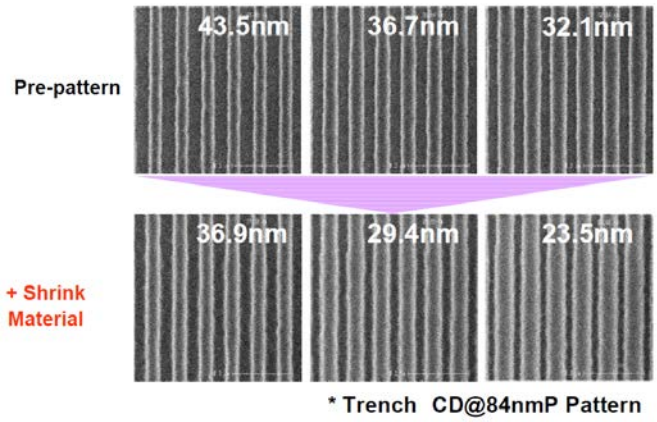

Figure 3. DRAM and FLASH facing density challenge.

3.4 DSA material

DSA is already on the ITRS roadmap. DSA has been proposed and studied for line, space or contact hole creation as well as for contact hole shrink, pattern repair, CDU improvement and pitch splitting. JSR has already demonstrated ca. 20nm transferred line patterns with our blend system in 2011. JSR has broadened the DSA research for blocked copolymer system as well as blended polymer system extensively as one of the future patterning solution. We have researched and

developed not only DSA materials but also guiding resist, neutral layer, and HM material for DSA process as package. We have already demonstrated various capabilities with our materials as shown in Figure 4 and 5.

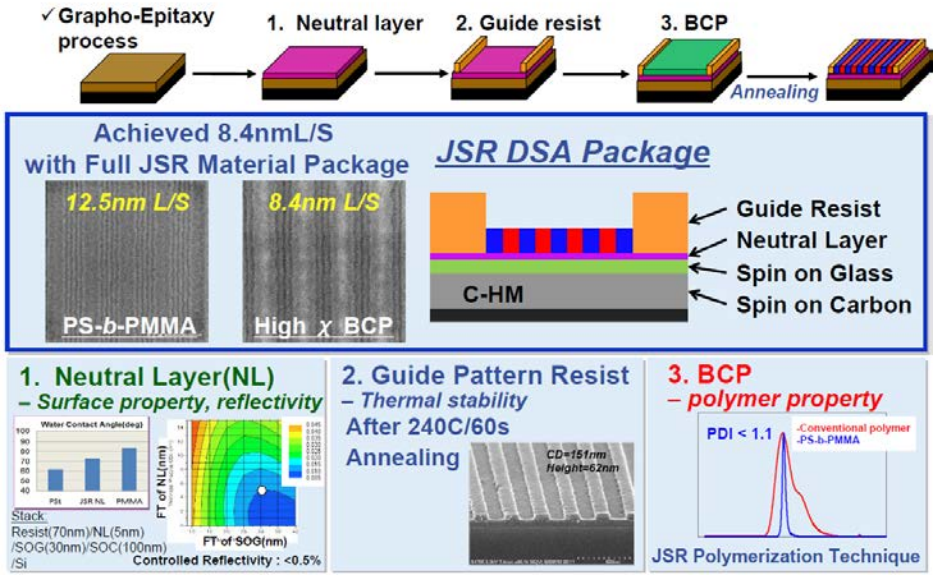

Figure 4. JSR's DSA BCP package and performance.

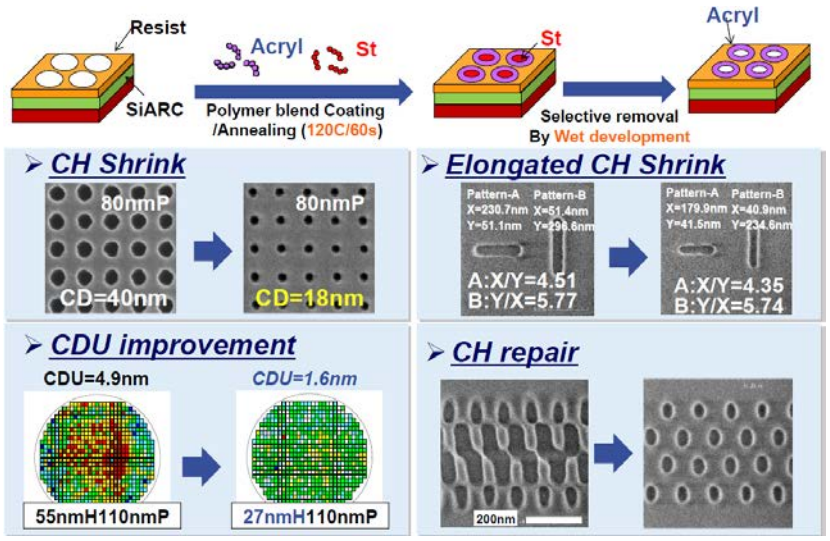

Figure 5. JSR's Blend DSA and performance.

3.5 Organic Spin-on Hardmask for EUV lithography

Resist film thickness has been thinner for newer generation mainly due to the collapse issue. Most advanced ArF immersion resists are now operated at less than 100nm film thickness often. However, EUV photoresist thickness needs to be further thinner like 50nm or less. For such a thin film thickness, HM is necessary to transfer the patterns. Each of the necessary materials in the EUV process should be optimized for its best performance. JSR has developed a package solution for EUV lithography as shown in Figure 6.

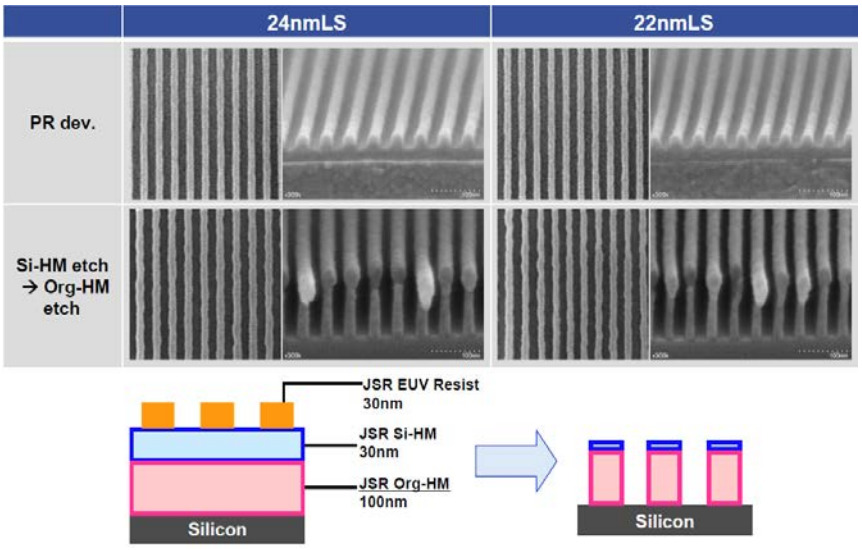

Figure 6. JSR's EUV hardmask package.

3.6 Spin-on Metal Hard mask(HM)

Double patterning or even quadruply patterning need multi-steps with multi HM materials stack formation. In addition to traditionally existing CVD type hard mask materials like nitride, oxide, and carbon deposited film, new hard mask materials have been studied to strategically differentiate etch selectivity from existing materials. Among many, metals can be good HM materials. JSR has studied and developed spin-on metal HM. Some examples are shown in Figure 7.

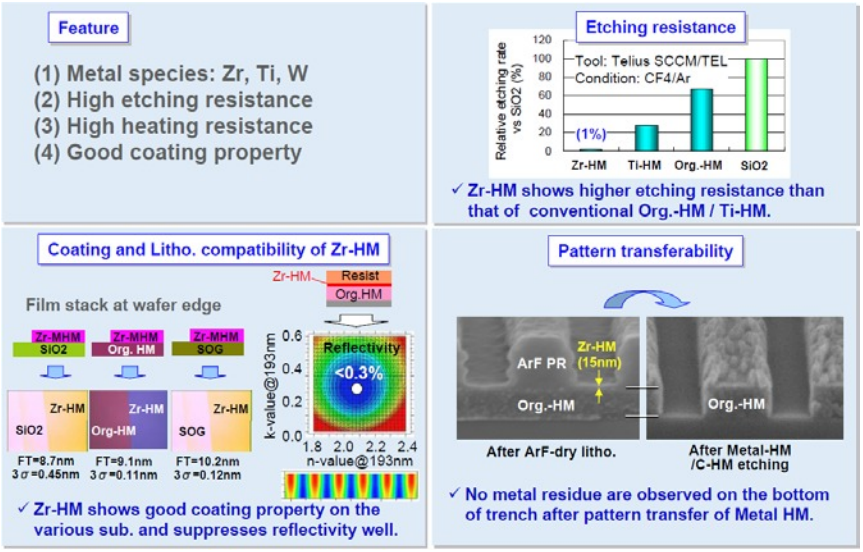

Figure 7. JSR's metal hardmask.

4. CONCLUSION AND FUTURE VIEW

Scaling requirements, device structure, and new types of architectures for new generation device with the limited single exposure capability will force us to keep using complicated multi-step patterning techniques or "tricks". New patterning

techniques will require newly developed, dedicated materials for tighter CDU and stricter defect control. 10nm or beyond device will continue to expand complications and need even more "tricks" than the current ones like device design, elements, process, and consumables. New devices and new application of the device like *in vivo* application will be continuously realized in the industry. To achieve the market's requirement, JSR will provide a series of the best advanced materials including photoresist, spin-on hard mask, top-coat, NGL material, packaging material, CMP material and so on.

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