Low Frequency Noise Behavior of Polysilicon Emitter Bipolar Junction Transistors - A Review

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ABSTRACT

For many analog integrated circuit applications, the polysilicon emitter bipolar junction transistor (PE-BJT) is still the preferred choice because of its higher operational frequency and lower noise performance characteristics compared to MOS transistors of similar active areas and at similar biasing currents. In this paper, we begin by motivating the reader with reasons why bipolar transistors are still of great interest for analog integrated circuits. This motivation includes a comparison between BJT and the MOSFET using a simple small-signal equivalent circuit to derive important parameters that can be used to compare these two technologies. An extensive review of the popular theories used to explain low frequency noise results is presented. However, in almost all instances, these theories have not been fully tested. The effects of different processing technologies and conditions on the noise performance of PE-BJTs is reviewed and a summary of some of the key technological steps and device parameters and their effects on noise is discussed. The effects of temperature and emitter geometries scaling is reviewed. It is shown that dispersion of the low frequency noise in ultra-small geometries is a serious issue since the rate of increase of the noise dispersion is faster than the noise itself as the emitter geometry is scaled to smaller values. Finally, some ideas for future research on PE-BJTs, some of which are also applicable to SiGe heteorjunction bipolar transistors and MOSFETs, are presented after the conclusions.

Key words: 1/f noise in bipolar transistors, low frequency noise, noise in scaled devices, impact of technology on noise performance, noise comparison, temperature effects, figure-of-merit, polysilicon emitter bipolar junction transistors

1. INTRODUCTION

Polysilicon emitter (PE) bipolar junction transistors (BJTs) are increasingly used in modern VLSI bipolar high-speed, high-frequency circuits. This is partly because the self-aligned process technologies used to fabricate PE-BJTs provides for a coordinated scaling of both lateral and vertical device dimensions. In this way, many device resistances and capacitances are reduced or suppressed, resulting in improved high-frequency performance characteristics. Also, the decreasing dimensions results in increasing unity-gain frequencies. This technology is therefore well-suited for applications in telecommunications or mixed-mode analog-digital integrated circuits because of its high-speed, high-current drive capability and low-noise properties.

PE-BJTs also provide significantly higher current gains compared to diffused junction BJTs primarily because of the thin interfacial oxide layer between the mono-crystalline and poly-crystalline emitter. Another technologically important reason is the compatibility of these devices with CMOS transistors to create BiCMOS technologies. The lower noise in PE-BJTs translates into lower noise circuits such as amplifiers, mixers and oscillators which are important in front-end transceiver circuits. However, as PE-BJTs are scaled to smaller dimensions, their low frequency noise (LFN) increases and for modern technologies, this can be a problem. For example, the low frequency is a serious design constraint in

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voltage-controlled oscillators (VCOs) because the LFN gets up-converted to phase noise causing spectral broadening. Low frequency noise in fact places a fundamental limit of the spectral purity of RF and microwave systems. It can affect both the power requirements of the circuit and the channel spacing in multi-channel wireless systems such as cell-phones. Low frequency noise can also be up-converted to affect the high-frequency performance of mixers, oscillators and amplifiers due to the non-linearity in the devices. Noise sets a lower limit for signal detection in electronic systems.

At present, there are many articles describing low frequency noise in polysilicon emitter bipolar transistors[1-40]. In many publications, for low frequencies below 1 to10 kHz, the noise is $f^{-\gamma}$ type, with γ typically in the 0.8-1.2 range, in which case, the noise is referred to as 1/*f* noise or sometimes flicker noise. There are also reports of γ values greater than 1.4. Others have reported on generation-recombination (*g-r*) noise in the same frequency range as 1/*f* noise, and even burst noise and random telegraph signal (RTS) have been observed. At frequencies greater than 1 to10 kHz, and depending on the biasing and device geometry, white noise dominated by shot noise in the base current and thermal noise in the parasitic base and emitter resistances are usually observed.

To date, most of the experiments reported are in which the base biasing resistance (R_{Bias}) is much larger than the total device input resistance R_{IN} (where $R_{IN} = R_B + r_\pi + (\beta + 1)R_E$ with R_B and R_E being the base and emitter resistances, $r_\pi = \Delta V_{BE}/\Delta I_B$) and h_{FE}, the current gain), suggest that the noise is associated with the base-emitter junction $_{I,i}$ and that it is fully correlated with the output noise $S_{I,o}$, for example $S_{I,i} = S_{I,o}/\beta^2$. Also, at medium to high base current densities that are typically used in analog integrated circuits, most experiments shown that the base current noise spectral density is proportional to the square of the base current, that is $S_{I_B} \propto I_B^2$.

2. WHY BJTS

An important advantage of PE-BJTs is the lower low-frequency noise (LFN) characteristics compared to similar CMOS transistors. In a recent publication[5] comparing the normalized noise characteristics of PE-BJTs with MOSFETs, as shown in fig. 1, the BJTs have about an order of magnitude lower noise than MOSFETs of similar active areas

For analog and radio frequency (RF) integrated circuit (IC) applications, high current gain (β) and Early voltage (V_A) products (βV_A), high unity-current gain frequency (f_T), high maximum oscillation frequency (f_{MAX}) and low LFN are required. Polysilicon is usually used as the emitter to enhance the transistor's performance by increasing h_{FE} to high values which are then reduced to acceptable values by increasing the base doping level to increase V_A, resulting in a high (βV_A) product.

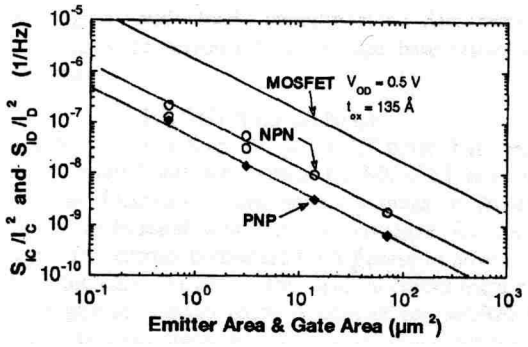

Fig. 1: Normalized collector and drain current noise spectra as a function of the devices active areas. For the MOSFETs, the gate over drive voltage was constant and for the BJTs, the BE voltages were the same. From ref. 5.

In contrast, MOS transistors usually have lower f_T and f_{MAX}, and higher low frequency noise for similar device areas and current levels, as shown in fig. 1. In fig. 2, we show very simple small-signal circuits of a BJT and a MOSFET in the common emitter (CE) and common source (CS) configurations, including the important noise sources for both low and high frequencies. These simple models will be used to derive simple formulas that can be used as a guide for analog engineers and designers to understand how the transistors' performance parameters are related to their electrical characteristics. The parameters for BJTs and MOSFETs are written with subscripts B and M respectively in the following five expressions.

$$\text{Transconductance: } g_{m,B} = \frac{qI_C}{kT} \text{ and } g_{m,M} = \sqrt{\mu C_{OX}^{*} \frac{W}{L} I_D} \tag{1}$$

$$\text{Unity current-gain frequency: } f_{T,B} = \frac{g_m}{2\pi(C_{BE} + C_{BC})} \text{ and } f_{T,M} = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{2}$$

Maximum oscillation frequency: $f_{max,\,B} = \sqrt{\dfrac{f_T}{8\pi R_B C_{BC}}}$ and $f_{max,\,M} = \sqrt{\dfrac{f_T}{8\pi R_G C_{GD}}}$ (3)

Output resistance: $r_{O,\,B} = \dfrac{V_A}{I_C}$ and $r_{O,\,M} = \dfrac{1}{\lambda I_D}$ (4)

Intrinsic voltage gain: $A_{\mu,\,B} = \dfrac{qV_A}{kT}$ and $A_{\mu,\,M} = \dfrac{\sqrt{\mu C_{ox}^{*}\dfrac{W}{L}I_D}}{\lambda}$ (5)

Because g_m of a bipolar is higher than g_m of a FET, the related parameters such as f_T and f_{MAX} are larger. Similar comparisons of other parameters can also be made from the expressions listed in the expressions above. Note that the expressions for f_T and f_{MAX} for both transistors are identical with appropriate interpretations of the capacitors and resistors. Also note that the two low-frequency circuits are identical.

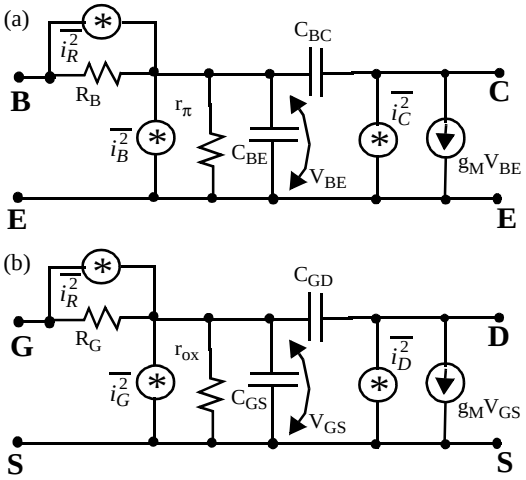

Fig. 2: Simple small-signal circuits with the main current noise sources of (a) BJT and (b) FET in a CE and a CS configurations are shown.

In fig. 2(b) at low frequencies, the noise source $\overline{i_G^2}$ is due to the gate current in modern MOSFETs since the gate insulator is very thin, less than a few nm. At high frequencies, $\overline{i_G^2}$ is the gate-induced noise due to the channel noise and it is important since it increases quadratically with *frequency.* Based on the small-signal circuit in fig. 2(a), for low frequencies, assuming that the capacitors are open-circuited, that the base is biased with a battery through a biasing resistance R_{Bias} and that a load resistance R_L and biasing battery are connected at the collector terminal, and that $R_{Bias} \gg R_B + r_\pi + (\beta + 1)R_E$ is the emitter resistance R_E is included, then the voltage noise spectral densities[6] measured at the base, **B** (S_{V_B}) and collector **C** (S_{V_C}) terminals, are

$$S_{V_B} = r_\pi^2 S_{I_B} + 2r_\pi Real\{S_{I_B I_C}\} \tag{6}$$

$$S_{V_C} = \beta^2 R_L^2 S_{I_B} + R_L^2 S_{I_C} + 2\beta^2 R_L^2 Real\{S_{I_B I_C}\} \tag{7}$$

$$Real(S_{V_B V_C}) = -R_L r_\pi(\beta S_{I_B} + Real\{S_{I_B I_C}\}) \tag{8}$$

$$\text{with } Imag(S_{V_B V_C}) = -R_L r_\pi Imag\{S_{I_B I_C}\} \text{ and } \Gamma_{V_B V_C} = \left|S_{V_B V_C}\right|^2/(S_{V_B} S_{V_C}) \tag{9}$$

In general, for the source biasing condition stated above, the coherence function $\Gamma_{V_B V_C} \approx 1$, so the noise sources at **B** and **C** are fully correlated and only S_{I_B} is dominant. In the case of modern deep-submicron MOSFETs with very thin gate oxides, it is tempting to state that the same expressions with the following changes are applicable

$$S_{V_B} \to S_{V_G};\ S_{V_C} \to S_{V_D};\ S_{I_B} \to S_{I_G};\ S_{I_C} \to S_{I_D};\ R_B \to R_G;\ \text{and } r_\pi \to r_{ox}. \tag{10}$$

However, this must be checked. An important point to emphasize is that with the continued down-scaling of the MOSFET oxide thickness, the current flowing through the gate oxide must be accounted for when analyzing their LFN. This also means that the gate noise and its correlation with the channel noise must be measured for proper LFN analyses.

3. MODELS

To date, there is some agreement among researchers that the low-frequency noise in PE-BJTs is due to fluctuations in the base current and it is of 1/*f* type. In some cases, especially for devices with very small dimensions, there is also generation-recombination (g-r) noise. The physical origin and location of the noise sources of 1/*f* and g-r noise are still active areas of research. Because of this, we briefly review, in this section, several models that have been used to explain measured low frequency noise spectral densities in PE-BJTs. In addition, we will explicitly discuss the expected normalized noise current spectral densities variations with physical, material, geometry and operating parameters such as oxide

trap density, oxide thickness, temperature, device geometry, oxide barrier height and surface capacitance. We do not discuss low frequency noise in PE-BJTs in terms of mobility fluctuations because most of the recent research shows that $1/f$ noise in PE-BJTs scales with the square of the base current I_B rather than linearly with I_B at normal biasing currents. However, for completeness, it is useful to state that in BJTs, there is also$1/f$ noise associated with the diffusion of carriers through the emitter-base space charge region, but this is usually much lower that the measured noise.

3.1. Two-step tunneling model

The two-step tunneling model[7] was used to explain the low frequency noise in tunnel diodes. In the first step, there is a recombination of carriers from the semiconductor bands into bound states at the SiO_2 interfacial layer next to the monocrystalline silicon by the Shockley-Read-Hall process. In the second step, there is elastic tunneling of carriers from these interface states into bound or slow states in the oxide that are located close to the interface. Based on these physical ideas, the current noise spectral density in a PE-BJT can be modelled as

$$\frac{S_{I_B}}{I_B^2} \approx \frac{q^4}{\ln\left[\frac{\tau(x_o)}{\tau(0)}\right] \cdot 2k\varepsilon_{ox}^2} \cdot \frac{N_T t_{ox}^2}{TA_E^* f}. \tag{11}$$

Here, N_T is the number of traps per unit area and energy interval ($cm^{-2}eV^{-1}$), t_{ox} is the oxide thickness and T is the absolute temperature. The tunneling time constant $\tau(x)$ with which the electrically charged states in the oxide communicate with the interface states is given by $\tau(x) = \tau_o \cdot \exp(\alpha x_o)$, with $\tau_o = 10^{-3}s$ and $\alpha x_o \approx 18$. An important aspect of this model is that A_E^* is a fraction of the emitter area because tunneling occurs preferentially through the thinnest parts of the oxide. This is important for PE-BJTs with non-intentionally grown oxides, since it is known from transmission electron microscopy (TEM) experiments[8] that this interfacial SiO_2 layer is indeed non-uniform in thickness.

3.2. Random walk model

In the random walk model[9], 1/f noise is generated by the random walk of carriers in interfaces via interface states. These randomly moving carriers interact with surface phonons to form polarons which have very low mobilities and are the source of flicker noise. However, as stated in ref. 9, a weak point of this model is the predicted very low mobilities of carriers in the interfaces. This model assumes that the slow states at the Si-SiO_2 interface are responsible for the noise and was used to explain experimental results in refs. 8, 10 and 11. Here, the noise power spectral density is

$$S_{I_B} = 0.1 \cdot \frac{I_S^2}{fA_E N_{IT}}, \tag{12}$$

where N_{IT} is the interface state density. The surface current is given by

$$I_S = I_{SO}\exp\left(\frac{eV}{nkT}\right) \text{ with } I_{SO} \approx \frac{ev_{th}\sigma n_i A_E N_{IT}}{2} \text{ and where } n\sim 2 \tag{13}$$

Using the normal expression for the base current, $I_B = I_{BO}\exp\left(\frac{eV}{mkT}\right)$ where $1 \le m \le 2$, (14)

it can be shown[9] that

$$S_{I_B} \Big/ \left(I_{SO}^2 \frac{I_B^{2m/n}}{I_{BO}^{2m/n}}\right) = \frac{0.1}{fA_E N_{IT}}. \tag{15}$$

3.3. Surface noise due to carrier density fluctuations

Surface $1/f$ noise due to carrier density fluctuations was discussed in ref. 12. This noise is due to the modulation of the oxide traps near the Si-SiO_2 interface to surface recombination via surface potential and fast surface states. If free carriers are captured by oxide traps through tunneling, then the capture cross-section σ of the traps is given by $\sigma = \sigma_o \cdot \exp(\theta x)$, where θ is a tunneling parameter and x is the tunneling distance. The $1/f$ noise is given by

$$\frac{S_{I_B}}{I_B^2} \sim \frac{kTN_T}{\theta A_S f}, \tag{16}$$

where N_T is the number of traps per unit area and energy interval ($cm^{-2}eV^{-1}$) and A_S is the surface area.

3.4. Tunneling-fluctuation model

The transparency fluctuation model discussed in ref. 13 assumes that Nyquist noise of the insulator layer modulates the barrier height and thus the tunneling probability of carriers. This model states that

$$\frac{S_{I_B}}{I_B^2} = \frac{1}{\left[1 + \sqrt{\frac{kT}{2\pi m_p}} T_{P,ox}\left(\frac{1}{s_m} + \frac{W_m}{D_m} + \frac{W_p}{D_p}\right)\right]^2} \cdot \frac{4\pi q k m_p \cdot \tan\delta}{3h^2} \cdot \frac{t_{ox}^3 T}{f\varepsilon_{ox} V_o A_E}, \tag{17}$$

with m_p being the effective mass of holes, $T_{P,ox}$ the tunneling probability for holes through the oxide layer, s_m being the hole recombination velocity in the metal, $W_{m,p}$ and $D_{m,p}$ being the width and diffusivity of holes in the monosilicon and polysilicon layers respectively, V_o the barrier height, tanδ the loss tangent of the oxide and ε_{ox} the dielectric constant of the oxide layer. The predicted temperature dependence of the normalized noise S_{I_B}/I_B^2 is not straightforward and has to be calculated based on the parameter values in expression (17). However, it is expected that S_{I_B}/I_B^2 will have a sub-linear dependence on temperature.

3.5. Tunneling-assisted trapping model

Here, the base current fluctuations are ascribed to surface noise from the low-frequency fluctuations of the surface generation-recombination base current component[14]. The noise is due to the dynamic trapping-detrapping of carriers into and out of slow states located in the spacer oxide at the periphery of the emitter-base junction. Based on these ideas, the base current noise is

$$\frac{S_{I_B}}{I_S^2} = \frac{q^4\lambda}{kC_{SC}} \cdot \frac{N_T}{T(P \cdot W_{SC})f}. \tag{18}$$

Here, P is the emitter periphery, W_{SC} is the width of the base-emitter (B-E) space charge region at the surface, λ is the attenuation tunneling distance of 0.1nm, C_{SC} is the semiconductor surface capacitance per unit area and N_T is the oxide slow state volume density ($eV^{-1}.cm^{-3}$). The surface recombination current I_S is given by

$$I_S = ev_{th}\sigma N_{IT} n_i \cdot e^{e\phi_S/kT} \cdot (e^{eV/2kT} - 1)\ . \tag{19}$$

and it was recently used to explain experimental results in ref. 11. Note that in this case, the surface recombination current is not the same as the base recombination current and it is difficult to calculate because of uncertainties in some parameter values. In ref. 8, it was assumed that $I_S = 0.5I_B$ and the other half of the base current could be due to recombination in the monosilicon emitter.

3.6 Superposition of G-R noise

Based on experimental results in refs. 1, 15, 16, 17 and 18, a noise model[19] for PE-BJTs based on a superposition of g-r noise, similar to that in MOSFETs according to the number fluctuation model was proposed. This model assumes that the trap energy levels E_T are uniformly distributed according to

$$dE_T \sim d(\ln\tau) = \frac{d\tau}{\tau}, \tag{20}$$

and the number of traps N_T is given by

$$N_T = N_{T,dec} \cdot \log\left(\frac{\tau_2}{\tau_1}\right), \tag{21}$$

where $N_{T,dec}$ ($\sim A_E$) represents the number of traps having τ_i in one decade. The normalized base current noise spectral density is then given by

$$\frac{S_{I_B}}{I_B^2} = \frac{K_F N^*_{T,\,dec}}{A_E f}. \qquad (22)$$

In eqn. (22), $N^*_{T,\,dec}$ is the number of traps per unit area per decade of frequency. Note that the parameter K_F is empirical and it depends on the operating and physical details of the transistor. An important consequence of this model is its ability to predict the relative noise level variation as the transistor size is scaled to very small emitter areas. This is shown in fig. 3.

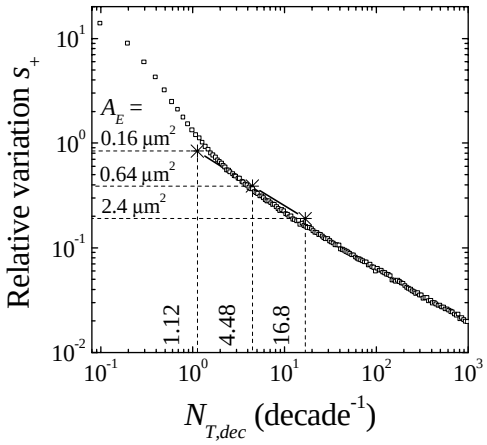

Fig. 3: Simulation of relative noise level variation as a function of $N_{T,dec}$ together with measured values of s_+ for different A_E fitted to the simulations.

3.7 Summary of 1/f noise models

Table 1 presents a summary of the expected dependence of the normalized current noise spectral densities on various technology, geometry and operating parameters. An additional model discussed in Refs. 20 and 21, based on noise generation in the E-B space charge region is also included. This model might be applicable to epitaxially aligned PE-BJT where there is negligible or no interfacial oxide present.

Model	N_T	t_{ox}	Temperature	Geometry	V_o	Expression
Ref. 7	N_T	t_{ox}^2	T^{-1}	A^{*-1}_E	--	(11)
Ref. 9	N_T^{-1}	--	--	A_E^{-1}	--	(15)
Ref. 12	N_T	--	T	A_S^{-1}	--	(16)
Ref. 13	--	t_{ox}^3	complex	A_E^{-1}	V_o	(17)
Ref. 14	N_T	--	T^{-1}	$(P_E \cdot W_{SC})^{-1}$	--	(18)
Refs. 15,16,19	N_T	--	complex	A_E^{-1}	--	(22)
Refs. 20,21	N_T	--	complex	A_E^{-1}	--	--

Table 1: Parameter dependence of the different 1/f noise models discussed.

4. EFFECTS OF PROCESSING TECHNOLOGIES ON LOW FREQUENCY NOISE

In this section, we discuss the effects of processing on the noise characteristics. This is important since different processing steps and technologies have different effects on the presence and properties of the interfacial oxide layer between the single-crystal silicon and the polycrystalline silicon emitter. In the discussions below, the following expression

$$S_{I_B} = \frac{K_F \cdot I_B^2}{f} \qquad (23)$$

with $K_F \propto 1/A_E$ will be used whenever possible. This will allow us to compare values of $K_F \cdot A_E$ in μm^2 as a figure-of-merit.

In refs. 10, 8, a study of the effects of processing on the noise characteristics of PE-BJTs was reported. It was found that the thickness of the ever-present interfacial oxide layer depends on the monocrystalline surface preparation and the annealing conditions. These are now summarized as follows.

- HF etch results in a thin non-uniform interfacial oxide ~0.4nm thick that is discontinuous. The thickness can vary from 0 to 0.8nm. See fig. 4(a).

- RCA surface clean results in a 1 to1.4nm thick interfacial oxide that is relatively uniform. See fig. 4(b).
- High temperature anneal (1000^{o}C) after the polysilicon deposition but before emitter implantation results in "balling" of the oxide layer in which the diameter of the sphere is ~8nm. See fig. 5(a).
- For sufficiently high temperatures (~1050^{o}C), there is epitaxial regrowth of the polysilicon layer. See fig. 5(b).

A schematic representation of the emitter structure after these four types of surface treatment[10] is shown in figs. 4 and 5. These cleaning procedures or heat treatment has a significant impact on the DC electrical characteristics and also the low-frequency noise characteristics.

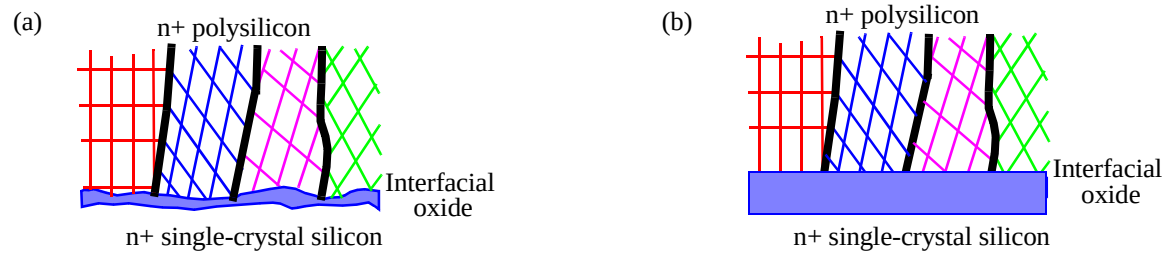

Fig. 4: Structure of the silicon dioxide interfacial layer between the monocrystalline and polycrystalline emitter after (a) RCA and (b) HF surface treatment. From ref. 8.

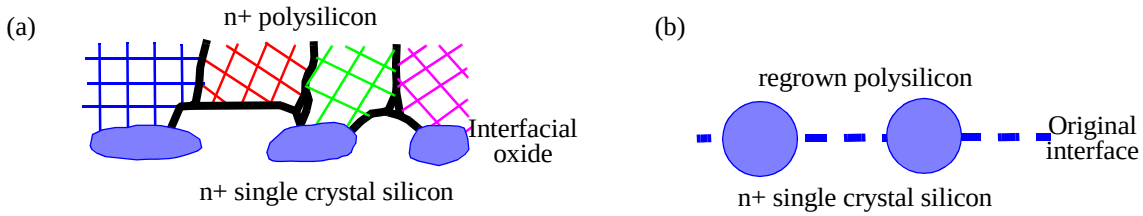

Fig. 5: Structure of the silicon dioxide interfacial layer between the mono- and poly-crystalline emitter after high temperature heat treatments. In (a), there is a high temperature preanneal to stress the oxide after poly-Si deposition but before the emitter anneal. In (b), there is epitaxial regrowth of the poly-Si if the temperature of the heat treatment is high enough. From ref. 8.

The relative variation of the noise voltage at 10 Hz for a 18x6μm^2 PE-BJT biased at I_C=0.2 mA is shown in the table 2. A fit to the experimental data showed that the interface state density was ~2x10^{11} cm^{-2} for the RCA cleaned devices. In addition, the following conclusions can be made about the noise in "treated" PE-BJTs[10,8].

- Noise in "balled" oxide transistors was considerably lower than in RCA cleaned transistors.
- Almost identical noise level was obtained for "balled" oxide and expitaxially realigned emitter. This implied that polysilicon has little or no effect on noise.
- Devices implanted with fluorine immediately after arsenic emitter implant had a noise reduction by a factor of ~3. Fluorine results in a reduction of the interfacial trap density without a break-up of the interfacial oxide layer, so the current gain is not changed much.
- Shallow emitter-junctions results in increase noise because the poly/monosilicon interface is in, or close, to the emitter-base depletion region which together with the large number of trapping states at the interface increases the noise. Non-ideal base current I_B are also observed in devices with shallow junctions.

The noise results from refs. 8 and 10 are summarized in table 2.

	RCA clean	**RCA Fluorinated**	**HF clean**	**Balled Oxide**	**Epitaxial alignment**
Noise voltage ($nV/\sqrt{Hz}$)	50	16	14	8.5	7
Current gain β	1300	1100	75	45	20

Table 2: Comparison of the noise voltage at 10 Hz and current gain in PE-BJTs with different surface treatments.

In refs. 22, 23 the effects of surface cleaning, polysilicon emitter thickness, emitter-base implant conditions, emitter geometry and temperature on the noise characteristics were discussed. It is known that silicon surface has a high affinity

for oxygen, resulting in the immediate formation of a thin layer of SiO_2, SiO, unoxidized Si, SiH and SiOH groups on the monocrystalline surface before the polycrystalline layer is deposited. When hydrous hydrofluoric (HHF) acid is used to remove the surface oxide and other contaminants, a highly reactive hydrophyllic surface is created. For anyhydrous HF (AHF) surface cleaning, the silicon surface is left fluorinated with less carbon contaminants and a higher degree of saturation of the silicon dangling bonds compared to the HHF cleaning. The results of current gain and noise characteristics of PE-BJTs subjected to these two types of cleaning, at I_B=1 μA and V_{CC} =5V, is shown in the table 3.

Surface Etch	β	$K_F \cdot A_E$ (μm²)
4 min. HHF	55	$2.7\text{x}10^{-9}$
10s AHF	65	$2.1\text{x}10^{-9}$

Table 3: Comparison of the DC and noise parameters for PE-BJTs with two types of surface treatments[22].

The effects of polysilicon emitter thickness on the noise characteristics of PE-BJTs was also studied[22,23]. Changing the polysilicon thickness t_{POLY} form 240nm to 360nm resulted in an increase in current gain from 50 to 75, but further increase to 400nm resulted in a current gain of 80. However, the noise parameter $K_F \cdot A_E$ in μm² remained almost the same at ~$3.8\text{x}10^{-9}$. The increase in t_{POLY} from 240 to 320nm results in an decrease in the hole current into the emitter contact because of the increase in the effective recombination velocity due to recombinations at the grain boundaries. The grains of polysilicon are typically 100nm wide, so the added recombinations due to dangling bonds and trapping sites at the grain boundaries decrease the base current and thus increase the current gain. However, recombination is saturated after 3-5 grains, so further increase in t_{POLY} does not result in an increase in current gain. The fact that $K_F \cdot A_E$ of the base current noise is relatively constant even though t_{POLY} increases indicates that the noise from the polysilicon layer is a negligible contribution to the base current noise. It is also a good method to change h_{FE} without affecting the noise characteristics.

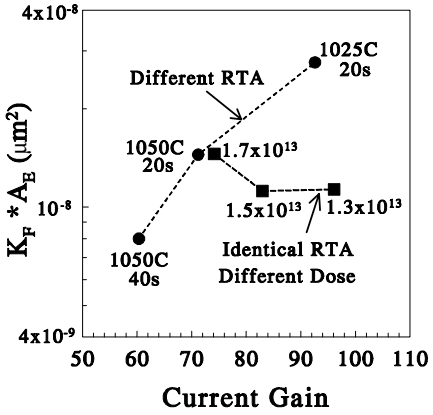

Fig. 6: Noise parameter $K_F \cdot A_E$ versus curre gain for PE-BJTs fabricated with differe base implant conditions. Here either the implant energy, implant dose, RTA time or RTA temperature was varied[22].

The effects of both implant dose and rapid thermal annealing (RTA) conditions on the noise characteristics of PE-BJTs was also investigated[22]. RTA is a technique commonly used to activate implanted species and to remove radiation damage. Compared to thermal annealing, RTA does not result in a redistribution of the dopants atoms and is therefore very suitable for devices of very small dimensions. For RTA, unless the temperature is high or the annealing time is long, most of the defects such as vacancies or interstitials that are created by implantation remains. The results are shown in fig. 6

From these measurements and simulations[22,23] the following conclusions could be made.

- As the emitter junction depth decrease, current gain and noise increases. This is due to the fact that as the junction moves closer to the mono-polysilicon interface, a larger number of minority carriers can reach the interface and interact with interface states. This also indicates the noise source is not in the emitter-base space charge layer.
- Decreasing base thickness results in increased gain and very little change in the noise. This indicates that the noise is not due to diffusion which is dependent on the base thickness.
- For identical RTA, the noise is almost constant, but current gain increases with decreasing base implant dose. This presents a good way to control the current gain without changing the noise behavior of PE-BJTs.

The effects of base width to change the breakdown voltage was also investigated[22]. The 5V devices had a narrower base width than the 10V devices, however, the noise parameter $K_F \cdot A_E$ in μm² was $5\text{x}10^{-9}$ and $6\text{x}10^{-9}$. This again indicates that the base width or diffusion did not play a significant factor in the base current noise.

In refs. 24, 25, an extensive investigation on low-frequency noise characteristics of various PE-BJTs was reported. For one set of devices, RTA was carried out for 10s at 1100°C to break up interfacial oxide layer or at 900°C for 20 min-

utes to leave it continuous. For the second set of devices, RTA emitter anneal at 1075, 1100 or 1125°C for 10s was carried out before As implantation. However, the noise spectra was only measured at 8 discrete frequencies between 1 and 100 Hz and even though it was stated that no g-r noise was observed, the spectra from low-impedance source resistance showed significant deviations from 1/f noise at 0.6 and 15 μA and at frequencies below 10Hz. Using the results presented in eq. (3b) of ref. 25, and for the D_{ox} variation between (1.6 and 2.6)x10^{15} atoms/cm^{-2}, then $K_F \cdot A_E$, is from $(3.4 \ \ to \ \ 26) \times 10^{-9} \mu m^2$ and this value was higher for furnace annealed samples. These oxygen doses correspond to t_{ox} from 1.6nm to 2.6nm. Also, if these results are extrapolated to zero oxide thickness, then for the same sized transistor (emitter area = 20x20 μm^2), the $K_F \cdot A_E \approx 0.16 \times 10^{-9} \mu m^2$.

The noise in these PE-BJTs[24,25] were interpreted in terms of the tunneling barrier fluctuations model because the noise increased with oxygen dose, was higher for FA than RTA devices and it varied as I_B^2. From experiments,

$$K_{ox} \cdot A_E \approx 1.6 \times 10^{-10} e^{5.36 t_{ox}} \mu m^2 , \tag{24}$$

where K_{ox} is the same as K_F except that it is now expressed as a function of oxide thickness t_{ox} in nm. Note that even though these experiments were interpreted in terms of the tunneling barrier fluctuations model, the expected t_{ox}^3 dependence presented in eqn. (17) was not obtained. Note also that the predicted value of $K_{ox} \cdot A_E$ is about an order of magnitude smaller than the lowest reported values of this figure-or-merit.

In ref. 26, three types of mono-silicon surface treatments were reported - a normal HF etch; a normal HF etch followed by a dry ozone treatment; and a normal HF followed by a wet ozone treatment. All wafers were subjected to a RTA at 1025°C for 20s. The calculated oxide (SiO and SiO_2) thickness were 0.47, 0.65 and 0.73nm respectively. For HF treatment, $K_F \cdot A_E \approx 2 \times 10^{-9} \mu m^2$ and for HF and wet O_3, $_F \cdot A_E \approx 20 \times 10^{-9} \mu m^2$. From analyses of the relationship between the barrier transparency and the LFN, it was concluded that the noise is generated by polysilicon/monosilicon hole transparency and another noise source. However, as stated in 26, the interfacial oxide layer is very thin, less that two atomic layers, and it is probably not uniform[26]. Also, the extracted $K_F \cdot A_E$ when plotted as a function of the calculated t_{OX} gave a stronger than t_{ox}^3 dependence.

The change in LFN due to changes in interface trap density that were obtained by different back-end process steps (N_{IT} from 3.7x10^9 to 9.2x$10^{10}$$cm^{-2}eV^{-1}$) was studied in ref. 27. The source of noise was identified as space-charge recombination current, surface recombination current in the neutral base, and base recombination current at the surface. The noise increased with N_{IT} and for large base currents greater than ~1 μA, the noise increased as I_B^2.

In ref. 28, LFN was reported for self-aligned PE-BJTs. However, the results were not separated into the different noise sources - 1/f and g-r noise sources - so it is difficult to compare. Frequency dependent noise varying as $f^{-0.99}$ to $f^{-1.98}$ were shown and the noise spectra themselves were "noisy". For the curve showing close to 1/*f* noise, the value of $K_F \cdot A_E$ was $\approx 5.2 \times 10^{-9} \mu m^2$. However, it was explained that the poly-Si/mono-Si interface which controls the base current is a key issue to both gain and noise. It was also speculated that some of the noise could be due to defects at the grain boundaries in polysilicon layer, but no experimental evidence was provided.

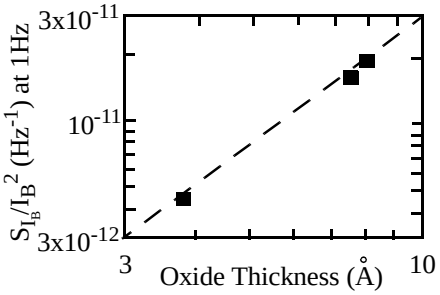

Fig. 7: Normalized noise versus oxide thickness. $K_F \cdot A_E$. From ref. 13.

The effect of hydrogen passivation by forming gas annealing (FGA) on the LFN in PE-BJTs was studied in ref. 29. It was shown that the noise magnitude decreases by a factor of 5 after FGA and also the corner frequency between 1/*f* noise and white noise decreased. The noise was modelled using the standard expression and the best value of the noise magnitude was $K_F \cdot A_E \approx 2 \times 10^{-9} \mu m^2$. In ref. 13, it was found that $K_F \cdot A_E \approx 3 \times 10^{-9} \mu m^2$, $S_{I_B} \propto I_B^2 / f A_E$ and that $S_{I_B} / I_B^2 \approx t_{ox}^2$ for t_{ox} from 0.4 to 0.8nm. This is shown in fig. 7.

In ref. 30, low-frequency noise was analyzed in terms of fluctuations in the height of the tunnel barrier which originates from the dielectric loss in the thin insulating films and a two-step tunneling process via traps in the insulating films. It was shown that both theories result in a noise spectral density given by

$$S_I = (\gamma T^{\delta} I^2) / f, \tag{25}$$

where γ and δ are constants and T is the temperature. Noise results were weakly temperature dependent and were analyzed in the framework of the fluctuations of the carrier tunneling probabilities through the interfacial oxide. The emitter area was not stated, but the $K_F \cdot A_E$ was approximately $2 \times 10^{-7} \cdot A_E \ \mu m^2$. This would be among the highest value reported, assuming that the emitter area is greater than $1\mu m^2$.

In ref. 31, the source of 1/f noise was assumed to be due to minority carrier recombination at the poly-monosilicon interface and at polysilicon grain boundaries in close proximity to the interface and minority carrier recombinations near to the poly-monosilicon interface, all of which have a I_B^2 dependence on noise. The emitter area was not stated but the $K_F \cdot A_E > 10^{-9} \cdot A_E \ \mu m^2$.

We can summarize the effects of processing on the noise performance with the following observations in table 4.

Reference	$K_F \cdot A_E$ **in** μm^2	**Effects causing changes to** $K_F \cdot A_E$
8, 10, 22	decrease	surface is cleaned with fluorinated treatment
22, 25	decrease	emitter junction depth is increases
22	decrease	base implant dose decreases
22, 25	decrease	RTA temperature or time increases
8, 10, 13, 24, 25, 26, 40	increase	interfacial oxide thickness increases
8, 10,22, 31	no change	increases of polysilicon thickness beyond 3-5 grain widths
22	no change	when base width increases; however, results were for limited changes.
29	decreases	when forming gas anneal is used to passivate hydrogen dangling bonds
8, 10	decreases	when emitter is recrystallized

Table 4: Variation of the noise figure-of-merit with technological and geometrical parameters.

5. TEMPERATURE EFFECTS

Most of the temperature dependent studies in PE-BJTs have been associated with g-r noise and efforts to extract the energy levels and capture cross-sections of traps[16,20,21,22,23]. However, in some of these publications, the 1/*f* noise was also extracted[22,23], and in the recent paper[11], the focus was on studying the temperature dependent of 1/*f* noise in PE-BJTs.

In fig. 8, the variation of K_F and current gain h_{FE} with temperature over a limited range is shown[22]. The base current at which these measurements were made was 2.5μA and the emitter area was $3.2\mu m^2$. Here, we see that the current gain increases with temperature primarily because of the of the increase in the minority carrier diffusivity in the base with temperature. However, K_F is practically independent of temperature. This result is similar to those reported in ref. 32 for PE-BJTs and SiGe HBT between -55 and +85°C; for SiGe HBTs in ref. 33 between 20 and +80°C; and for PE-BJTs in refs. 34 and 35 between 22 and +85°C.

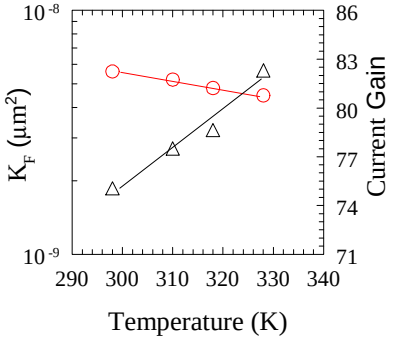

Fig. 8: K_F and current gain versus temperature for PE-BJTs from a 5V process[22].

In ref. 11, it was found that the base current noise power density S_{I_B} of npn transistors at temperatures between 198 and 247K varied inversely (but rather weakly) with temperature. However, from measurements, $S_{I_B} \propto I_B$, so the results were analyzed in terms of tunneling assisted trapping involving slow oxide states in the space-charge region at emitter surface periphery. Using the results presented in ref. 11, the value of $K_F \cdot A_{Sur}$ was found to be

$$K_F \cdot A_{Sur} = \frac{S_{I_B}}{I_S^2} \sim 8 \times 10^{-4} \mu m^2 . \tag{26}$$

At higher temperatures from 247 to 347K, the variation of S_{I_B} with temperature increased, remained constant or even decreased[11], depending on the surface recombination current. Here, the surface recombination was extracted from

the Gummel characteristics which is different from how it was determined in refs. 10, 8. It is believed that the surface current is not easy to calculate[9,10,11,14] (see eqns. (13) and (19) above) since some of the parameters are not easily determined. Therefore, more research is required to fully understand LFN in PE-BJTs as a function of temperature.

6. NOISE IN ULTRA-SMALL BJTS

From experimental results of several groups, it is known that the 1/*f* spectral noise density of the base current fluctuations at normal currents where the Gummel characteristics are ideal, and is given by

$$S_{I_B} \propto I_B^2 \text{ and } S_{I_B} \propto \frac{1}{A_E} . \qquad (27)$$

However, when the emitter areas are scaled to very small values below 1μm^2, generation-recombination noise appears and if the total low frequency noise spectra from several devices are averaged, then 1/*f* noise results with a magnitude equal to that of a larger area PE-BJTs scaled appropriately by the factor A_E^{-1} . The low-frequency noise spectra differ in both magnitude and characteristic frequency of the g-r center for each ultra-small emitter area PE-BJT.

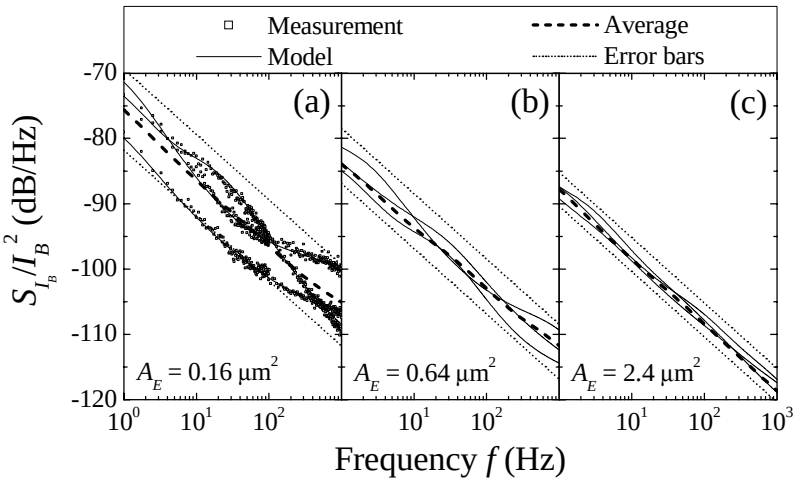

Fig. 9: Normalized base current noise spectral density for three PE-BJTs of different emitter areas[15]. The squares in (a) are the measured values while the solid lines are modelled values according to (28). The thick dashed lines are the average spectra from 8 PE-BJTs and the dotted lines are error bars calculated according to a confidence level >95%.

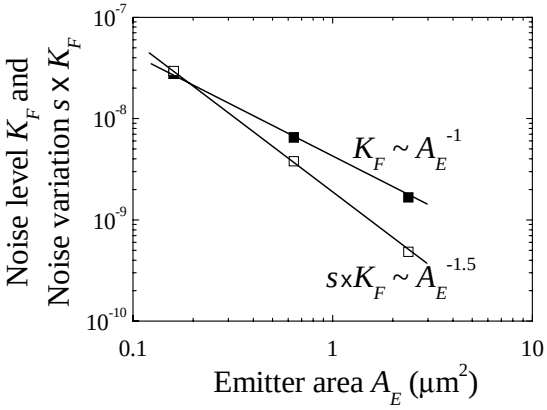

Fig. 10: Variation of the SPICE parameter K_F with emitter area A_E and the parameter $s \times K_F$ with A_E. From ref. 15.

The above results are also similar to what has been observed for MOSFETs of similar gate area in which both g-r noise and random-telegraph signals due to the capture and emission of carriers by a single interface trap, appear. These observations show that the trapping-detrapping processes in the interfacial oxide layer play an important role in the low-frequency noise formation in the PE-BJTs studied. It also indicates that noise due to the fluctuation of the tunneling probability originating form the interfacial Nyquist noise is unlikely since this model does not account for g-r noise. Finally, the noise results can also be used to qualitatively estimate the density of traps N_T which is responsible for 1/*f* noise.

An example of the normalized equivalent input noise spectral density for npn transistors with emitters areas from 0.16 to 2.4μm^2 is shown in fig. 9. Here, its is assumed that the total pink noise is a sum of 1/*f* noise and g-r noise according to the expression

$$S_{I_{B,j}} = \frac{K_{F,j} I_B^2}{f} + \sum_i \frac{B_{i,j} I_B^2}{1 + (f/f_{ci,j})^2} . \qquad (28)$$

where the subscript *j* refers to the *j*th sample. $B_{i,j}$ and $f_{ci,j}$ are the noise level and corner frequency of the *i*th trap respectively. Fig. 9 shows an example of noise spectra from identically processed PE-BJTs in which the average spectra from 8 transistors is 1/f noise and the product of $K_F \cdot A_E \approx 4.3 \times 10^{-9} \mu m^2$. The fact that all three transistors have the same $K_F \cdot A_E$ values indicate that the dominant sources for the low-frequency noise for transistors with small and large emitter

areas have the same origin. This is in agreement with the earlier results in refs. 17 and 18 for PE-BJTs from a different manufactures and over a larger range of emitter areas.

Based on these experimental results, a new formulation for the modeling the noise using the SPICE-type expression was proposed as

$$S_{I_B} = \frac{K_F I_B^2}{f}(1+s) + 2eI_B, \quad (29)$$

$$\text{with } s = 10^{\pm k\sigma_{dB}/10} \quad (30)$$

and where the parameter k depends on the confidence probability selected and for k=2, the confidence probability is above 90%. Fig. 10 shows the variation of K_F and the low-frequency variation $s \times K_F$ calculated from eqn. (30) with k=1. The important new conclusion is that the noise variation scales as $A_E^{-1.5}$. This has profound implications for the use of ultra-small emitter geometry PE-BJTs in analog ICs with differential inputs where matching is a serious design issue. To better appreciate this point, fig. 11 shows the average value of K_F (solid squares) and its lower (open circles) and upper (open triangles) values based on experiments of 8 sets of PE-BJTs at each A_E value.

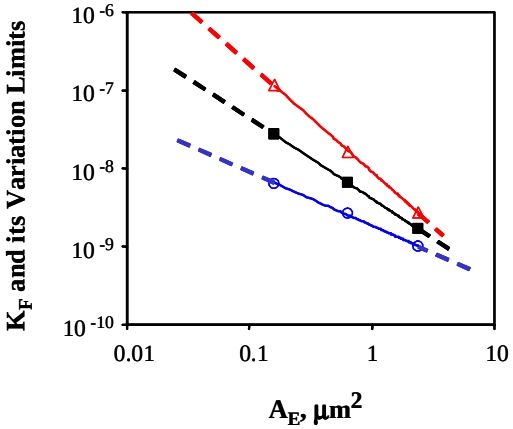

Fig. 11: K_F and its upper and lower variations as a function of emitter areas.

7. HOW TO COMPARE LOW-FREQUENCY NOISE RESULTS?

In this section, we summarize recent low frequency noise results obtained in PE-BJTs, some of which have been discussed qualitatively above. A simple way to motivate the discussion is to examine the expressions corresponding to the different theories above and to normalize the base current noise spectral density to I_B^2 at 1Hz, for example. What remains after this normalization will be referred to as a number representative of the normalized noise magnitude. However, since many experimental results report that S_{I_B} is inversely proportional to emitter area, we will use the following as a figure-of-merit, the product $K_F \cdot A_E$. In addition, some comments to describe some important details of the transistors are included in table 5.

Reference	$K_F \cdot A_E$ in μm^2	Comments
5	1.1x10^{-7} - npn 6x10^{-8} - pnp	A_E from 0.56 to 70μm^2. 1/f and g-r noise observed. BiCMOS technology with very large $\beta \cdot V_A$ products of 20,000 (pnp) and 4000 (npn) and f_T's of 6 and 4 GHz.
13	8.4x10^{-9}(t_{ox}, 0.4nm) 2x10^{-9} (t_{ox}, 0.8nm)	Furnace annealed for emitter drive-in at 1173K for 30 mins. Junction depth varies from 57 to 71nm.
14	2x10^{-8}	Self-aligned CMOS compatible technology used to make PE-BJT
15,16	4.3x10^{-9}	Small A_E from 0.16 to 2.4μm^2 used. N_T estimated >6x10^{8}cm^{-2}.
17	6.4x10^{-9}	A_E from 0.28 to 16.8μm^2. N_T estimated >3x10^{8}cm^{-2}and f_T was >15GHz. Self-aligned double poly-Si technology.
22	2x10^{-9}(AHF) 1x10^{-9} (RTA)	AHF etch was used to clean the mono-Si surface before poly-Si deposition RTA at 1050^{o}C for 40s. Quasi-self-aligned BiCMOS technology used.
25	1.3x10^{-9}	0.5μm single poly-Si technology with quasi-self-aligned E-B technology. This low FOM was for RTA at 1100^{o}C (very high).
26	2x10^{-9} 0.7x10^{-9}	First result was for quasi-self-aligned technology without recrystallized emitter. Second had the emitter recrystallized.
29	1.5x10^{-8} (before) 2x10^{-9}(after)	Transistors from self-aligned technology *before* and *after* forming gas anneal. A_E from 0.8 to 30μm^2, f_T >10GHz and RTA at 1000^{o}C for 10s.
28	5.2x10^{-9}	Self-aligned technology. Most spectra had significant g-r components.

Table 5: Summary of figure-of-merit $K_F \cdot A_E$ for PE-BJTs from different research groups.

Reference	$K_F \cdot A_E$ in μm^2	Comments
30	$2\text{x}10^{-7}*A_E$	S_I has a weak power-law dependence on temperature. Oxide layer was 1.4nm and standard RCA surface clean was used.
31	$10^{-9}*A_E$	Postulated that primary source of noise is due to majority carrier transfer through the polysilicon grain boundaries.
36	$1.5\text{x}10^{-8}$ (unmasked) $7.5\text{x}10^{-9}$ (masked)	Different emitter technologies. Quasi-self-aligned process. Surface HF cleaned. Wide range of device geometries studied.
37	$4\text{x}10^{-9}$	Single poly in BiCMOS process. Measurements over 3 decades in current.
38	$2.3\text{x}10^{-9}$	Commercial npn BJTs from Motorola.
34	$1.6\text{x}10^{-9}$ (npn) $1.4\text{x}10^{-9}$ (pnp)	Non-self-aligned complementary bipolar technology with junction isolation. For npn, BV_{CEO}~85V and f_T ~2GHz and for pnp, BV_{CEO}(pnp)~95V and f_T ~1.6GHz. A very low-noise, high-voltage, high-frequency technology.
39	$8\text{x}10^{-9}$	Different numbers of C, B and E stripes. Many areas studied.

Table 5: Summary of figure-of-merit $K_F \cdot A_E$ for PE-BJTs from different research groups.

8. CONCLUSIONS AND SUGGESTIONS FOR FUTURE RESEARCH

In this paper, we have presented motivations on why PE-BJTs continue to be of great interest and use to analog and radio frequency integrated circuit designers. This is primarily because of its many advantages that have been highlighted with simple expressions using a simple equivalent circuit model. A careful review of many of the existing theories used to explain low-frequency noise results was presented. In particular, the expected dependence of the normalized current noise spectral densities on various technological, geometry and operating parameters for each of the theory was explicitly shown and discussed.

A review of the important noise results from most of the major research groups was then presented and this was succinctly summarized by using an appropriate figure-of-merit, $K_F \cdot A_E$. The effects on $K_F \cdot A_E$ of different processing conditions such as RTA time or temperature, type of anneal such as furnace anneal or forming gas anneal, the thickness of the interfacial oxide layer and the polysilicon layer thickness was discussed. This is useful for it provides valuable information to device technologists interested in optimizing the noise and ac performance of these transistors.

The effects of temperature of the noise performance was then discussed. However, the discussion and conclusion is quite limited since there are very few publications on the subject. The important subject of noise in ultra-small emitter areas PE-BJTs was reviewed. Based on careful experiments with transistors from different laboratories, it was shown that there is significant dispersion in the measured low frequency noise characteristics as the transistors are scaled to ultra-small dimensions. This could be a major limitation for future use of these transistors in analog circuits, especially those circuits with differential inputs such as mixers or oscillators where low-frequency noise is already a serious concern. A model based on superposition of g-r noise was proposed to explain both the low-frequency noise results as well as the noise dispersion measured.

Finally, we returned to the topic on how to compare the noise results from different research groups. Based on the observation that most publications report that the input noise spectral density scales quadratically with the base current, the previous figure-of-merit mentioned was used to compare the noise magnitudes. From this comparison, it seems that the best PE-BJTs in bulk silicon technology have $K_F \cdot A_E$ that are ~10^{-9}μm^2.

Since this is a review paper, it is perhaps worthwhile to end with some suggestions for future research. These are now presented in no particular order.

- First is the origin of noise in ultra-small PE-BJTs that can statistically have no traps or defects in either the interfacial oxide layer or periphery. This is based on the assumption that N_T ~10^9cm^{-2} that has been obtained.
- Second, the effects of increasing dispersion with decreasing emitter areas requires further study. This together with the increase in LFN, the dispersion will limit the signal-to-noise ratio or bit-error-rates in communication systems using small A_E transistors.
- Third is temperature effects. This study should include temperature effects on both noise and DC electrical characteristics so that good physical explanations of the results can be attempted. This is also because the published results do not all agree.

- A fourth area for study is low current and voltage bias effects on the noise characteristics. This will become increasingly important since the push in wireless and to some extent wired circuits is for lower operating powers. This is interesting since the operating principles of the transistor can change if the bias is low enough - for example recombinations currents become dominant rather than diffusion currents. How this will be affected by device geometries or operating temperatures has not been studied?
- A fifth area of study is to investigate in detail which model can explain the experimental results properly. This will involve measurements on PE-BJTs with different technology, geometry and operating parameters and conditions. It should also be useful to develop a trap-assisted tunneling theory to explain the low-frequency noise in PE-BJTs with interfacial oxide, similar to what has been previously done for resonant tunneling diodes[41,42].
- A sixth area of study will be to develop a proper figure-of-merit (*FOM*) based on the low-frequency noise and other performance parameters. Some suggestions for this has been proposed[43], but more work is required. Examples of performance parameters to be considered are - low-frequency noise corner frequency f_c, unity-current gain frequency f_T, maximum ocillation frequency f_{MAX}, collector-emitter breakdown voltage BV_{CEO}, Early voltage V_A, current gain, linearity measures such as the third order intercept point *IIP3*. In addition, the dependence of the *FOM* on operating conditions such as bias currents or tempertaure, and on technology parameters such as base width or interfacial oxide thickness requires study.

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