Optical Lithography with and without NGL for Single-Digit Nanometer Nodes

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ABSTRACT

This presentation addresses the challenges to pattern single-digit nanometer nodes. Next generation lithography such as Extreme UV, Multiple E-Beam Direct Write, may or may not help to meet the challenges. Optical lithography may still be needed for all layers, in combination with NGL for relevant layers, or not at all. The consideration will be based on necessary requirements such as overlay accuracy, resolution, and defects. However, even if all these requirements are met, only a satisfactory cost can dictate the application in high volume manufacturing. Some considerations on costs will also be presented.

Keywords: Optical lithography, next generation lithography, single-digit nanometer nodes, overlay, resolution, defects, EUV, Multiple e-beam, Multiple e-beam direct write

1. INTRODUCTION

In the 1970s the minimum feature size in lithography was in single-digit micrometers. Four decades later, it is advancing to single-digit nanometers. There are 3 orders of magnitude in dimension shrinking in just four decades and is quite impressive. However, reaching single-digit nanometers is not easy, even more so, to advance further.

There are many challenges. The most difficult one is overlay accuracy. In the past, overlay followed reduction in feature size by tightening mechanical and metrological precisions. However, we are facing mechanical limits and requirement of sub-nanometer measurement precisions. In addition, non-lithographic tools and processes contribute to overlay errors. There are contributions from the mask and the lens as well. In this paper, detractors of overlay are discussed, their solutions suggested.

Second to overlay accuracy, reduction of the minimum feature size, i.e., increase of resolution, is still very difficult. Most resolution enhancement techniques, such as phase-shifting masks, removal of the zeroth order component in the illumination, optical proximity corrections, optimization of NA and sigma, suppression of multiple reflections and stray light have been fully developed. Wavelength reduction have converged to ArF light (193 nm dry wavelength, 134 nm immersion wavelength) and EUV light (13.5 nm wavelength). The numerical aperture peaks at 1.35 for ArF water immersion and at 0.33 for EUV lithography. To reduce the image pitch further, multiple patterning with and without spacers has to be used. What are the implications? How far can it go? Once the high-resolution aerial image is achieved with either ArF immersion lithography, EUV lithography, or multiple e-beam direct write (MEB DW), the resolution is gated by the resist. In this paper, the limits posed by the aerial image of ArF immersion lithography, EUV lithography, and MEB DW are compared. The impact of resist blur is shown as well as the resist development goal.

Just like overlay accuracy, defects cannot be readily scaled. Negligible defects of the present generation can become severe defects for the next generation. Defects can be induced by lithography and non-lithography tools, lithography and non-lithography processes, from the mask, and from the incoming materials. In this paper, defects are given a careful look and the defects from all three lithography systems are discussed.

Last but not least, the cost of the three lithography systems is compared in product settings of the 10-nm and the 7-nm nodes to give the readers a feeling of the cost impact of the lithography systems.

Two single-digit nanometer nodes, 7-nm and 5-nm are used to quantify the overlay accuracy, resolution, defect, and cost targets. Typical specifications are given in Table 1. SMO denotes single machine overlay; and MMO, multi

Table 1. Typical node specifications.

	7-nm	5-nm
Half Pitch (nm)	15	11
SMO (nm)	1.5	1.1
MMO (nm)	2	1.5
Defect density per layer	<1	<1
Cost Increase from the last node	1.15~1.4	1.15~1.4

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machine overlay. These specifications are just reasonable speculations, not the specification of any semiconductor manufacturing company.

This presentation is an extension of the presentation[1] given at the Micro and Nano Engineering Conference in 2014.

2. OVERLAY ACCURACY

Unlike resolution, overlay accuracy is mechanical and metrology limited. In addition to overlay error contributed from lithography tools and processes, it can also be worsened by non-lithographic causes. Two examples are given here.

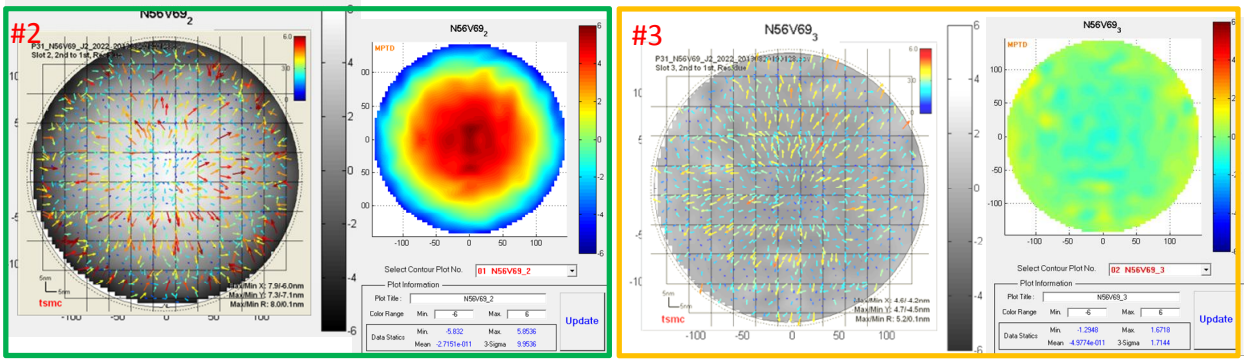
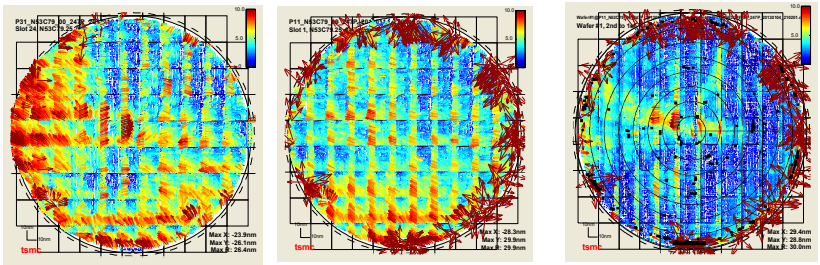


Fig. 1. Wafer #2 has a TiN layer which was skipped for wafer #3. The warpage was measured with a Zygo interferometer showing a range of 11.6 μm and 2.96 μm respectively. The overlay errors are 8 and 5.2 nm.

2.1 Warped wafers

Wafers often go through high temperature processes, resulting in warping caused by thermo induced stress. The features on the wafer follow the warped surface. When the wafer is flattened by the wafer chuck, these features move laterally as a function of warpage. Figure 1 shows the correlation of wafer warpage with overlay errors from a wafer with a TiN layer and another wafer without TiN. The overlay error induced by the warpage caused by the TiN deposition is 2.8 nm.



(a) (b) (c)

Fig. 2. (a) and (b) are overlay maps after the 1st and the 10th pass through the contaminating tool. Figure 2(c) is the contamination map from an optical microscope.

2.2 Backside contaminated wafers

Wafers can easily be contaminated at the backside from non-lithographic processes such as etching or chemical mechanical polishing. When chucked down, the top surface is bent, causing defocus and overlay error. Figure 2 shows the overlay error induced this way. The wafer was made to pass through the same contaminating tool ten times for correlating the increase of contamination to the increase in overlay error. Figure 2(a) shows the overlay vector map after the 1st pass and (b) after the 10th pass. Figure 2(c) is a view of the contamination from an optical microscope.

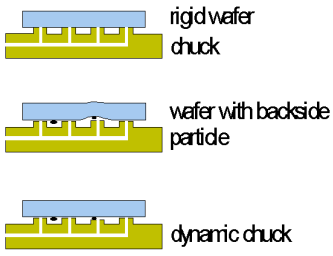


Fig. 3. (top to bottom) rigid wafer back referenced chuck; Sane chuck distorting a contaminating wafer; Dynamic front-referenced chuck.

2.3 Front reference chuck to improve overlay accuracy

Wafer warpage and contamination are perennial problems with past nodes. It is quite difficult to keep the wafer absolutely clean and undistorted. We propose a front referenced wafer chuck with dynamically adjustable surface

topography to yield to the particles at the wafer backside. Figure 3 shows three situations (a) Wafer-bottom referenced rigid chuck holding a clean and flat wafer (b) Same chuck but the wafer front surface is bent due to backside contamination. (c) Dynamic front-surface referenced chuck mitigating the effects of backside contamination.

2.4 High-order overlay corrections

Irregular wafer conditions above produce high-order nonlinear distortion requiring many high-order correction terms to reduce the overlay error. Figure 4 shows the overlay vector map of a nonlinearly distorted wafer. Using only 6 linear terms results an overlay residue of ±3 nm, which can be improved to ±1 nm using additional 12 high-order terms. The out-of-spec percentage improved from 1.5%~2.7% to 0~0.15% in 9 wafers. This type of overlay error is difficult to correct with rigid mask and lenses. Multiple e-beam maskless lithography enables high-order dynamic overlay corrections to deal with such situation.

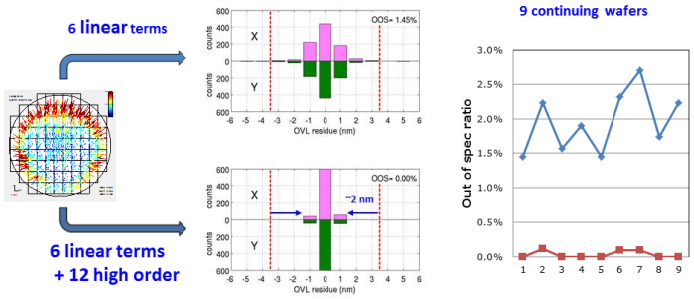


Fig. 4. Overlay accuracies with and without high-order corrections.

2.5 Mask contributions

In addition to controlling the placement errors on the mask, the flatness and bending of the mask also have to be controlled. For optical lithography, the lack of flatness from pellicle mounting can contribute to overlay errors but it is much smaller than the effects from lack of flatness on a EUV mask. EUV using a reflective mask, oblique illumination, an extremely short wavelength is ultrasensitive to lack of flatness. The flatness irregularity can be broken down into a map of longitudinal displacements of the mask pattern that translate to lateral displacement of the image, leading to overlay errors. The equation describing the relationship of the lateral displacement and the lack of flatness has been reported in an earlier article[2].

Eq. 1 $$\delta x'_{lat} = (2/m)\ \delta Z_{long} \tan\theta,$$

where m is the reduction ratio of the imaging optics; θ, chief ray angle; δZ_{long}, mask translation in the longitudinal direction. From Table 1, the single machine overlay tolerance is 1.5 nm. Allowing $1/\sqrt{2}$ of the total overlay tolerance for mask flatness variation, then $\delta x'_{lat}$ =1.06 nm. Substituting m = 4 and θ = 6° sets δZ_{long} to 20.2 nm. Hence, the flatness of EUV mask has to be within 20 nm for the 7-nm node. For the 5-nm node, with SMO=1 nm, the EUV mask flatness has to be better than 13.5 nm. In comparison, a very good mask for immersion lithography is specified for 500-nm flatness.

Mask flatness irregularity may be induced by substrate flatness, chucking errors, contamination of the mask, and stress. Naturally, maskless lithography systems are free from mask contributions to overlay error. In addition, the mask overlay budget can be waived to enlarge the wafer budget.

2.6 Elimination of overlay budget for mask

Maskless lithography systems can allocate the entire CDU and overlay budget to the wafer, instead of having to share the budget with the mask. This is a significant advantage in improving the overlay accuracy.

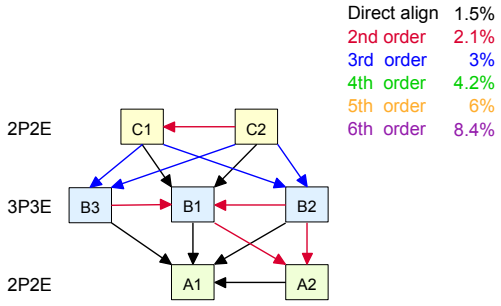


Fig. 5. Overlay tree of 2P2E aligned to 3P3E on 2P2E. Indirect alignments up to the 3rd order are present.

2.7 Contribution from multiple patterning

Because the NA and wavelength of immersion tools are fixed, multiple patterning is used to reduce pitch after the 28-nm node. The extra masking inevitably leads to indirect alignment. When many multiple patterning layers are aligned to each other, there can be higher-order indirect alignment. Figure 5 shows the situation of aligning a 2P2E layer to 3P3E which is aligned to another 2P2E layer. As high as 3rd order alignment is

produced, worsening the overlay accuracy by 2X. The most straightforward remedy is to use 1P1E. However, mixing 1P1E with multiple patterning layers cannot alleviate the problem. Figure 6 shows the situation of aligning a 1P1E layer to the stack in Fig. 5. Even though a 1P1E layer is used, 3rd order alignment is still present. To take advantage of 1P1E, all critical alignment layers have to be 1P1E. Therefore, all critical alignment layers have to use EUV, MEB DW, or a mixture of them.

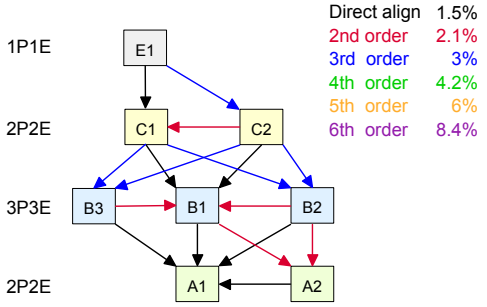


Fig. 6. Overlaying a 1P1E layer on multiply patterned layers cannot eliminate high-order alignments.

2.8 Self-aligned processes

To overcome the mechanical limitation in overlay, self-aligned processes have to be developed. A well-known self-align process[3] is shown in Fig. 7. After the poly-Si gate, shallow trench isolation, source and drain are formed. The self-aligned silicide is produced by depositing a layer of the desired metal, such as Ti or Ni, to react with Si at elevated temperature. After the silicide is formed, the unreacted metal is removed selectively with an etch solution. No masking is needed to form the self-aligned silicide in the source and drain.

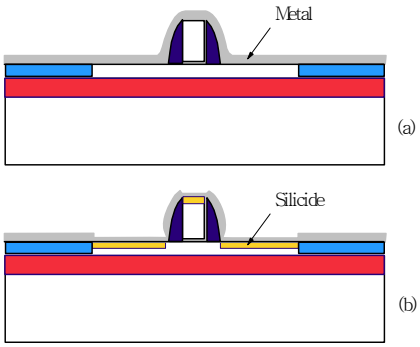


Fig. 7 Self-aligned silicide process

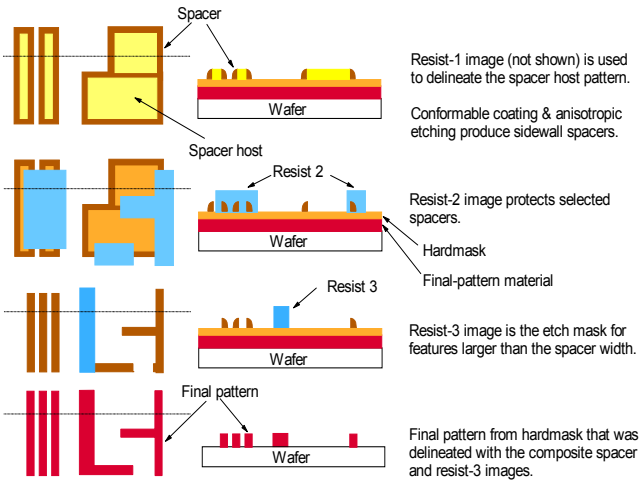


Fig. 8. The spacer technique to double resolution.

The spacer technique is also a self-aligned process. It is shown in Fig. 8. The sidewall spacers are self-aligned to the mandrels to form higher-resolution patterns. Removal of the mandrel and cutting of the loops are often necessary.

We need to develop many new self-aligned processes to meet the need of the ever tightening overlay accuracy.

2.9 Overlay-immune designs

There is no reason that overlay friendly circuit designs cannot be made. Designers should realize the mechanical limit of overlay accuracy and help to reduce the dependency on it. An example of overlay-immune design is to split the via layer according to the split of the metal layer that is to be aligned upon. Cross alignment between the split patterns[4] is removed.

3. RESOLUTION

3.1 Immersion lithography

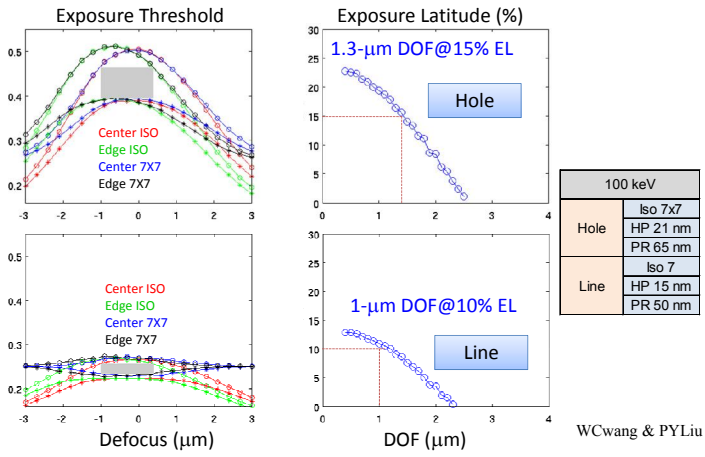
The resolution of ArF water immersion lithography peaks at NA=1.35 at the 193-nm ArF wavelength. The resolution of photon-based imaging systems is governed by the scaling equation,

Eq. 2 $$W = k_1 \bullet \frac{\lambda}{NA}$$

Where W is the half pitch of the feature to be printed; k_1, the resolution scaling coefficient; NA, the numerical aperture of the imaging lens; λ, the imaging wavelength. With NA and λ fixed, the only possibility to increase resolution is by reduction of k_1. With much work and accumulated experience, the industry can reduce k_1 to <0.3. Even though the absolute limit of k_1 is 0.25, it is quite impossible to reduce it further from 0.28, i.e. 40 nm half pitch. Similarly, the ultimate limit of the NA in the ArF water immersion system is 1.44 but it is not wise to increase it beyond 1.35. The lens will be very difficult to design and extremely expensive to build, not to mention the possibility of losing depth of focus (DOF) and field size, thus decreasing the productivity of the immersion scanner. The industry has manufactured circuits with immersion scanners at resolutions exceeding the capability of these scanners, by resorting to pitch splitting using the multiple patterning technique, the spacer technique, or a combination of them. The tradeoff is throughput and process complexity. There are unexpected advantages with the pitch splitting technique.

3.2 EUV lithography

EUV lithography uses λ=13.5 nm at NA=0.33. It is impossible to reduce the wavelength further with limited time, resource, and positive experience to draw upon. Because of higher level of stray light, less accurate optical precision, oblique chief ray, limited resolution enhancement techniques, and 3D masks, the difficulty of imaging at k_1<0.4 is no less than k_1=0.28 in ArF immersion imaging, leading to 16.2 nm half pitch, slightly larger than the required 15 nm for the 7-nm node shown in Table 1. EUV lenses with NA>0.33 have been discussed[5] but it is not wise to use higher NA EUV lenses. Similar to immersion lithography, the DOF and field size will suffer, losing process window and productivity, and necessitating new tools for the next generation. It is better to depend on multiple patterning, the spacer technique, or a combination of them to improve resolution just as in the case of immersion lithography. The tradeoff is throughput and process complexity just as multiple patterning in immersion lithography



Resist scattering and 10-nm blur by acid diffusion are included.

Fig. 9 Simulated processing window of L/S and hole patterns for the 7-nm node. These are the common window of isolated and dense patterns at the edge and the center of the e-beam column.

3.3 MEB DW lithography

E-beam imaging has the potential of extremely high resolution and large processing window. Figure 9 shows simulated imaging results from a 100 keV, 80X reduction e-beam column design for use in the REBL system[6]. The imaging current per column is 1.5 μA, sufficient to support more than 85 wph for holes, using 3x36 columns. The processing window is 1.3 μm DOF at 15% exposure latitude for holes and 1 μm DOF at 10% exposure latitude for lines and spaces. These windows are common window of dense and isolated patterns at the edge and the center of the e-beam column[7, 8]. With immersion lithography and EUVL struggling with DOF in the sub-hundred nm regime, having micrometer level DOF is a luxury.

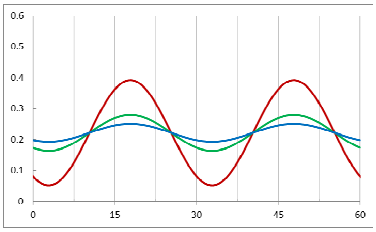


Fig. 10. Simulated EUV image intensity of 30-nm pitch gratings at resist blurs=0, 7, and 9 nm. The pitch of the image is 30 nm.

3.4 Resolution limit post by resists

Resist blur has become a key limiting factor on resolution for the 7- and the 5-nm nodes. Even though Fig. 9 shows that a 10-nm resist blur can support the 7-nm node in MEB, it is more difficult for EUVL. Figure 10 shows the image intensity distribution[9] from a 0.33 NA lens at λ=13.5 nm. The image contrast rapidly

drops when the resist blur is 7 or 9 nm. For the most critical layers in the 7-nm node, we may have to use EUV double patterning unless the resist blur can be kept below 5 nm. For the 5-nm node, MEB DW also requires resist blur smaller than 10 nm to facilitate single patterning. The situation is summarized in Table 2.

Resist blur	Pitch			
	30 nm		22 nm	
10 nm	EB: Single patterning	EUV: Double patterning	EB: Double patterning	EUV: Double patterning
5 nm	EB: Single patterning	EUV: Single patterning	EB: Single patterning	EUV: Double patterning

Table 2. Impact from resist blur.

The resist thickness is also a limiting factor. The height-to-width ratio in the resist image is generally capped at 3:1 to prevent resist collapse from the drying process[10] during development. For a 10-nm feature, a mere 30 nm of resist thickness has to serve as an etch mask. The etching resistance has to be managed or the adhesion of the resist has to be increased to use a higher aspect ratio to support etching.

Line width roughness (LWR) is also of great concern. Using the same image under the same processing condition, there is a tradeoff between LWR and the EUV exposure dosage as seen in Fig. 11. A higher dosage reduces the LWR at the expense of throughput, thus, cost. The curve can be moved to the left for better LWR only by increasing the image contrast, using the spacer technique, or directed self-assembly.

In summary, the resist blur, thickness, sensitivity, and LWR have to be suitable for the 7- and the 5-nm nodes.

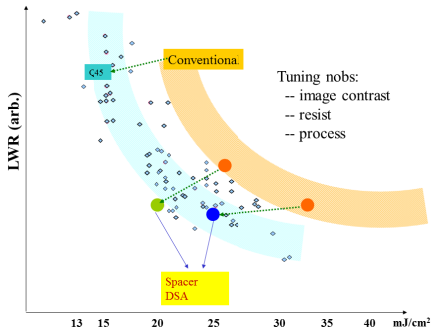


Fig. 11. Tradeoff between LWR and resist sensitivity

4. DEFECTS

Like overlay accuracy, defects do not scale as predictably as resolution and the specification on defects follows the advance of each node. The discussion on defects can be separated into two parts: Defects from mask and defects on wafer.

4.1 Defects on Mask

4.1.1 Defects in mask blank

It is extremely rare to find defects on mask blanks for optical lithography. The spec is zero. EUV lithography is a different story. Because of the extremely short wavelength and the reflective mode, a longitudinal surface irregularity of 13.5/4=3.4 nm can cause a π shift. This irregularity can be in the EUV mask substrate as well in the multi-layer for reflection. As of 2014Q4 the average count for defect size 23 nm and larger is 34 per blank[10]. There is still room for improvement. Many of these defects can be mitigated by globally shifting the mask patterns to maximize their coverage. Figure 12 shows mitigation of EUV mask blank defects using this scheme. The effectiveness of this scheme is dependent on the mask pattern density. There is a higher chance of success with contact and via layers.

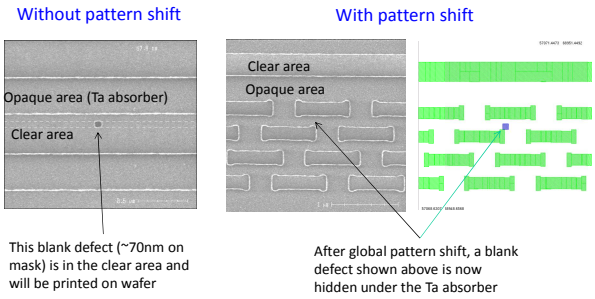


Fig. 12. Global mask pattern shift to mitigate EUV mask blank defects.

4.1.2 Defect repair

Similar to mask writing, repair of patterned absorber is not much different between optical and EUV lithography systems. Figure 13 shows some sample opaque and clear defects on EUV masks[11]. The mask images before and after repair are shown, as well as the wafer image from the repaired mask. Defects from patterned absorbers are manageable.

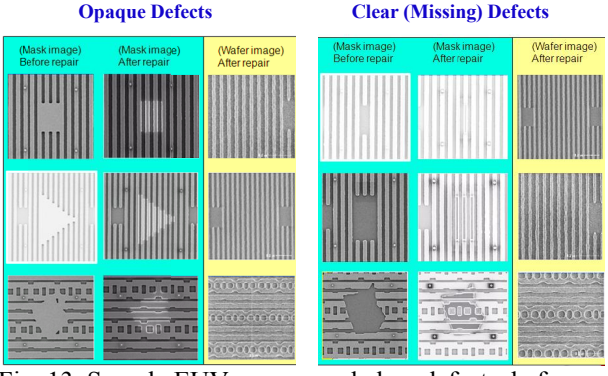


Fig. 13. Sample EUV opaque and clear defects, before and after repair.

4.1.3 Defect build up

During mask loading and unloading from the EUV scanner, the mask carrier, or any other equipment, during exposure or other processes, the mask can be contaminated. Figure 14 shows[12] a 1-μm size particle attached to the mask during step-and-scan exposure. The 1st 16 fields had clean wafer images. At the 17th field, a particle appeared and its image repeated through the rest of the fields. This type of defect build up occurred many times. The material has been found to be Sn or Ru. Hence, EUV pellicle is necessary. Pellicle life under intense EUV radiation and pellicle mounting stress causing overlay errors are challenges.

Another type of mask defect is contamination at the back side of the mask substrate[11], as shown in Fig. 15. If this defect is not removed before chucking, there is a higher probability of removal failure. The particle removal efficiency drops from 89% to 72% after chucking. Backside contamination on masks can cause overlay error and loss of DOF.

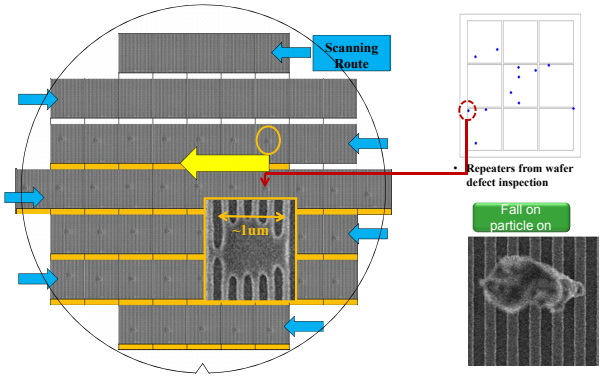


Fig. 14. A micrometer-size particle deposited on the EUV mask during scan-and-repeat exposure.

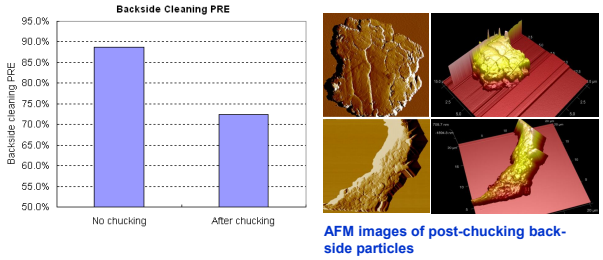


Fig. 15. Particle removal efficiency of chucked and unchucked masks with backside particle.

4.1.4 Defects on maskless masks

The REBL MEB maskless system also has a mask contamination problem. Even though it does not replicate a mask image, it demagnifies the dynamic image on the dynamic pattern generator (DPG) just the same. Any particle falling on it can potentially produce a repeating defect. The REBL team was aware of this defect potential and had incorporated the time delay and integration (TDI) mode [13], as shown in Fig. 16. The sensitivity to contamination on the DPG is reduced with redundancy. First, 5 levels of grey is used to define the position of each graphic element on wafer. Each bit is determined by a pixel on the DPG As the pixel is turned on and off dynamically while the wafer is being scanned in the horizontal direction, the exposure accumulates to define the position of the graphic element on wafer. An additional level of grey is used to even out the differences between DPG pixels at different positions in the DPG and at different columns. This 2^6 array is repeated four times to further increase the redundancy. Hence, there is a total of 2^8 bits in the array to define the position of a pixel. When one bit is missed, only 1/256 exposure is affected. To make the exposure of one data point exceed 10% exposure latitude, there has to be 26 bad pixels lined up in the scan direction. Therefore, the 2^8 redundancy makes the REBL system much less sensitive to contamination. The 80X reduction ratio of the REBL column also helps to screen out small defects.

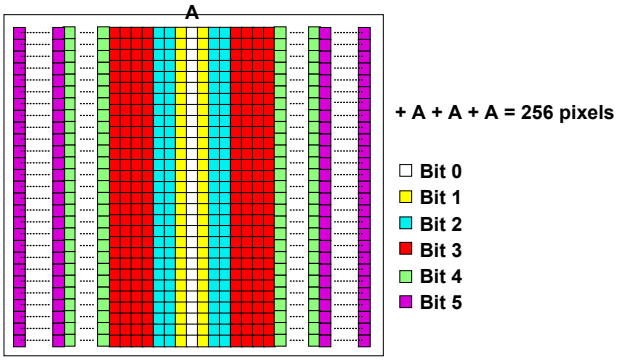


Fig. 16. TDI scheme makes the DPG much less to contaminations.

4.2 Defects on Wafer

Defects on wafer can be classified by their cause. They can be already on the wafer before lithography just as defects imbedded in the mask blank. They can be process induced, tool induced, or material induced. Unfortunately, defects on wafer cannot be repaired as those on mask, due to complexity and cost.

Defects generated by non-lithographic processes such as etch, CMP, etc. can cause overlay error and reduce DOF as discussed in Sections 2.1 and 2.2. They may cause electrical problems in addition to just lithography problems.

For defects deposited on wafer during exposure on immersion tools, improper wetting and bubble generation from the immersion fluid may be defect sources but they have long been taken care of, except for tightening of defect size specification in each node advance or for increasing the scan speed. For EUVL and MEB DW, the electrostatic chuck may be a defect getter. In the former, there may be presence of tin in the exposure chamber to be trapped electrostatically. Because the defect generation mechanisms are different, it is incorrect to assume that nPnE in immersion lithography produces more defects than 1P1E in EUVL or MEB DW.

Defects generated from other lithographic processes such as coating, baking, and drying, have equal opportunity of occurrence for immersion lithography, EUVL, or MEB DW. They are becoming more and more difficult to mitigate.

Defects in incoming materials are also of concern. The materials suppliers have to upgrade their factory on defect level in their materials for each node.

5. COSTS

To sustain Moore's law, the price per die of the next generation has to be worth the gain in performance and density from the existing generation. Otherwise, there is no incentive for the customer to move on to the next generation. One cannot count on the customer absolutely needing the gain in performance at uncontrolled cost. The price consists of the cost of manufacturing the die as well as the profit margin required for all providers to sustain their business. The cost of manufacturing consists of more than lithography costs. However, we will focus on lithography cost in this paper. We now discuss the cost of immersion lithography, EUVL, and MEB DW.

5.1 Cost of optical lithography

The cost of optical lithography and that of immersion lithography in particular, can escalate in several ways. Obviously, it is directly related to the number of masking layers required of the next generation. Starting from the 20-nm node, the number of masking layers increases faster than the historical trend, due to multiple patterning. The number of mask splits for each circuit layer can increase beyond two, for a particular geometry. This increase is alarming not only for cost but also for process complexity and overlay accuracy. One of the important tasks for lithography engineers is to innovatively reduce the number of masking layers without trading off density and electrical performance.

Another cost contributor is the exposure tool. Even though the NA of tools does not increase any further, the overlay performance of the exposure tool has to improve, making the tool price increase substantially. Also, the increase of wafer throughput is slowing down. The historically effective cost reduction scheme is becoming less effective.

Due to the requirement of better CD uniformity and low defect level, the wafer processing tracks as well as the processing materials such as resists, under layers, etc. also become more costly.

5.2 Cost of EUVL

The most significant cost factor in EUVL is wafer throughput. The EUV exposure tools are inevitably more expensive than optical tools, immersion scanners included. The wafer throughput is also lower than that of optical tools. One saving grace is that single patterning in EUV can replace multiple patterning, which has a turnover point at about 3P3E with EUV tool delivering 250 W to produce 100 wph. Of course, when EUV 2P2E has to be used, as discussed in Sec. 3.4, the turnover point moves to 6P6E of optical tools. To be precise on the turnover point, we have to consider tool maintenance and utility costs, EUV mask blank cost, mitigation of blank defects, reparability, contamination, mask cleaning life time, cost and lifetime of pellicles, as well as the cost of mask inspection and repair verification tools.

A yet undetermined cost component is wafer throughput gated by resist sensitivity and shot noise. Delineating small 2-D features with acceptable CDU requires exposure dosages in the order of 60 mJ/cm^2, which was predicted theoretically[14] and experienced in the lab. This dosage is 3 times higher than the rated dosage and can severely impact EUV productivity, thus cost. Reference 14 concluded that 1000 W of EUV power is necessary to make EUVL cost effective.

5.3 Cost of MEB DW lithography

For MEB DW the cost differentiator is number of columns and the corresponding data path for each column, because of the sheer number of columns required. It is desirable to make 108-column MEB exposure cost for L/S per move similar to that of EUVL at 125 W source power. For holes, because of a lower pattern density, the MEB exposure cost should be made roughly half of that of EUVL at 250 W source power. Under these conditions, the exposure cost of MEB DW is approximately equivalent to that of 2P2E in immersion lithography.

For less critical layers, the space-charge limit of the MEB column is relaxed, enabling higher current for imaging. Also, shot noise is less severe, allowing resist of higher sensitivity. Wafer throughput is increased. It is economically feasible to use MEB DW for all circuit layers, critical and non-critical[1]. In addition to economy, the overlay accuracy, mask cost and cycle time savings are also advantageous.

5.4 Mixing immersion, EUV, and MEB layers

Mixing nPnE immersion L/S exposure with MEB cutting and MEB hole imaging is the most cost-effective way to pattern wafers. When n becomes unbearably costly, an economical EUV L/S exposure can be mixed with MEB cutting and hole imaging. This plays into the high-throughput potential in MEB DW on low pattern density layers and the relatively higher resist sensitivity that can be used for EUV L/S patterning. As discussed in Sec. 5.2, delineating holes and cutting layers can significantly reduce EUV exposure productivity. There is one concern. It is more difficult to mitigate mask blank defects for the L/S layers. The EUV/MEB mix requires mask blanks to reach a usable defect level.

Overlay accuracy is also of concern with mixing of these tools. A more than economical desired number of EUV layers may have to be incorporated to attain the required overlay accuracy. It is less of a concern with the Immersion/MEB mix because high-order overlay matching is feasible for MEB DW as shown in Sec. 2.4.

5.5 Cost comparison

Following the considerations above, three case studies were performed to compare ArF water immersion, EUVL mixed with ArF immersion at two different EUV source power levels, and MEB mixed with ArF immersion, as shown in Table 3. Costs are compared to that of the 10-nm node. The most expensive situation can be 2.4 times the cost of the 10-nm node and is unacceptable for the Moore's law of economy. Case 3 is more cost effective, even though still costly in terms of economy of node advancement. Only MEB-ArFi approaches an acceptable cost target according to Table 1. EUV-ArF_i at 250 W has the opportunity of being slightly less expensive than pure ArF_i, if the exposure dosage can be kept at the rated 20 mJ/cm^2.

Cost of all layers	10-nm	7-nm			
Litho tool	ArFi	ArFi	EUV-ArFi		MEB-ArFi
Power at IF	N/A	N/A	125W	250W	N/A
Case 1	1	2.10	2.40	2.00	1.70
Case 2	1	1.74	2.18	1.81	1.58
Case 3	1	1.49	1.56	1.45	1.40

Table 3. Cost comparison for the 7-nm node.

6. CONCLUSION

Four major challenges to extend lithography to the 7-nm node and beyond are discussed. Overlay accuracy is the most difficult to handle. In addition to typical contributors to overlay errors, multiple patterning adds to the difficulty and it cannot be resolved by mixing single patterning with multiple patterning. Non-litho processes such as wafer warping or backside contamination can induce overlay errors. Fundamental solutions to overlay errors consist of self-aligned processes, overlay-error-immune designs, maskless lithography to eliminate error contributions from the mask, a front flattened wafer chuck, and using single patterning for all masking layers. For EUV, keeping the mask flatness below 20 nm is necessary. With MEB DW, its high-order correction capability can be taken advantage of.

For ArF immersion lithography, the resolvable pitch is 80 nm at k_1=0.28. It is not wise to reduce it further by increasing the NA or reducing k_1 due to high cost and marginal process window. Pitch splitting with multiple patterning is used to pattern smaller pitches. Similarly the resolvable single-exposure pitch of EUVL is 32.4 nm at k_1=0.4 and NA=0.33. It is not wise to increase the NA or reduce k_1 but multiple patterning is preferred for the same reasons. Fortunately the DOF of MEB DW is an order of magnitude larger than that of the other two technologies. Even so, if the resist blur cannot be

brought down to 5 nm or below, double patterning is needed for MEB DW at the 5-nm node and for EUV at the 7- and 5-nm nodes. Resist LWR and pattern collapse also have to be improved.

Defects do not readily scale just as overlay accuracy. Defects on EUV mask blank have to be mitigated with global absorber pattern shift. Fall-on defects have to be kept out of focus with a pellicle. Pellicle durability and mounting stress have to be taken care of. The DPG on multiple e-beam systems can also be susceptible to contaminations. The TDI imaging scheme and large demagnification alleviate the problem. Defects on wafer can be produced by the electrostatic chuck in EUVL or e-beam lithography as well as from improper wetting and bubbles in immersion lithography. The latter has been overcome within acceptable scanning speed. Defects can also be problematic for incoming materials; resist baking, developing, and drying. Defects generated from non-lithographic processes can be even worse.

Cost escalation is a serious issue. Multiple patterning increases exposure cost many folds at each circuit layer requiring multiple patterning. The number of circuit layers also increases for newer generations. High tool cost, low productivity, and expensive infrastructure besiege EUVL on cost and technical difficulties. MEB DW cost is heavily dependent on the cost of columns and electronics as well as pattern density. There are cost effective schemes to mix ArF immersion with MEB DW. Mixing ArF immersion with EUVL can also help to reduce cost, if other EUVL concerns are addressed.

Overlay and process window considerations favor MEB DW. Eliminating the mask removes many defect possibilities. It favors maskless systems. In addition, MEB DW has the potential to be the cost champion. Unfortunately, there is insufficient industrial momentum to develop MEB DW systems. Many of the reasons are not technically related.

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