Teaching Undergraduate Students Integrated Photonics and Fabrication Through Research

Donald Witt[a,b], Enxiao Luan[a], Kashif Masud Awan[a,b], Jaspreet Jhoja[a], Lukas Chrostowski[a,b]
[a]*Electrical and Computer Engineering, University of British Columbia, 2332 Main Mall, Vancouver, BC*

[b]*Stewart Blusson Quantum Matter Institute, 2355 East Mall, Vancouver, BC, V6T 1Z4, Canada*

ABSTRACT

An innovative undergraduate level Nanofabrication course with a focus on photonics is proposed. This course challenges the definition of what constitutes an undergraduate class in a research-intensive university. Namely, instructor and teaching assistants (TAs) propose a moderately challenging graduate-level research project that has not been previously published; challenge the Team, consisting of the students, with the TAs and instructor, to research during the class, as a Team; have the Team collaborate on writing a research paper with the goal of submitting it to an archival journal. Through this process, students learn the course content and experience how research is conducted.

Keywords: Nanofabrication course, thermo-optic switch, doped heaters, spin-on dopant

1. INTRODUCTION

Silicon photonics is a rapidly evolving field with applications in communication, quantum computing and health care [1]. To prepare students to enter this field, and the field of nanotechnology in general, the University of British Columbia offers an undergraduate level nanofabrication course (ELEC 463). This year, we decided to incorporate a research project into the course content.

Several learning outcomes for the students were proposed. The first objective was for them to learn the core content of the course. The second objective was to for them to experience how research is conducted within the specific discipline. The goal behind this objective was to give students experience with how research is conducted that they normally wouldn't receive during their undergraduate education. Part of this objective was to have them co-author a collaborative journal paper. This gives students experience in a vital aspect of research. The third objective was to use design reviews and peer reviews to improve upon the content everyone produces. This was important for multiple reasons. First, it improved the student designs to ensure that everyone ends up with functional designs. Secondly, it improved the content of the research paper. Finally, design and peer reviews will be used throughout the students' future careers and this process gave them initial experience with these processes. Another part of this preparation was having the students' present their research results in a public setting. The final objective was to submit the collaborative manuscript to a journal for publication.

The course project was in the field of photonics integrated circuits (PICs) implemented using silicon photonics technology. A key component in most potential applications of silicon photonics are electrically-active devices. To fabricate these devices, ion implantation is typically used to implant the dopants. Unfortunately, this process is too expensive and time consuming for rapid prototyping within a single-semester undergraduate course. We proposed using spin-on dopant [2] and electron beam lithography as a low-cost alternative. Spin-on dopant is commonly used to make electronic devices[3,4] and solar cells[5,6] but, to the best of our knowledge, has not been used to fabricate active silicon photonic devices. Students were given the objective to perform a design-fabricate-test cycle of a thermo-optic 2x2 switch based on a Mach-Zehnder Interferometer. The objective was to develop a fabrication process for creating partially-etched silicon rib waveguides on a silicon-on-insulator wafer, doping them to create doped heaters which act as thermal phase shifters [7], and creating metal contacts. The novel process developed used a spin-on dopant, as opposed to the standard ion implantation technique. Students performed automated tests of the passive photonic devices and manual electro-optic characterization of the devices.

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2. STUDENT DESIGNS

The course started with the students learning the core content of the course needed to be able to fabricate successful designs. The students learned the basics of silicon photonics and nanofabrication. As part of this, they learned how to simulate their designs using commercial software: Lumerical MODE [8] for simulating optical waveguides, and Lumerical INTERCONNECT [8] for simulating the photonic circuits. This was done through both traditional classroom instruction and online modules hosted on the edX platform. The goal was for the students to be able to understand and design a thermo-optic 2x2 switch based on a Mach-Zehnder Interferometer.

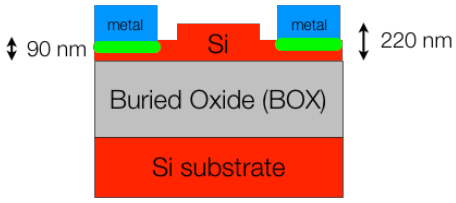

Figure 1. Cross section of the process. One can see the 90nm slab of silicon along with a 220nm thick waveguide. The N++ contact dopant is highlighted in green.

Figure 2. An example of a thermo-optic switch based on a Mach-Zehnder Interferometer. The waveguides that make up the interferometer are visible in red. The N++ contact dopant that forms the heater is visible in purple. The metal is visible in green.

Once they had the required understanding to design a successful device, they began making their layout. They did this using the open source layout editor KLayout [9] and the SiEPIC-EBeam-PDK process design kit [10]. After the students had produced their initial designs, they conducted a design review to check for mistakes and improve their work. Once this process was complete, the fabrication portion of the course began.

3. FABRICATION

Since this year's course involved an entirely new and untested fabrication process, several chips were made. The first chip was sent out for fabrication with Applied Nanotools [11]. This chip contained purely passive photonic components. This was done to ensure the students would have measurements to report and would learn the core course content even if the in-house fabrication did not work. Two chips were fabricated with the students so that each lab section would be able to follow the fabrication steps. This also allowed for more parameters to be varied and for any lesson learned during the first lab section to be applied to the second.

The first step in the fabrication process was to pattern the devices using our state of the art Jeol-8100FS electron beam lithography system. Students first observed how their designs were fractured in GenISys BEAMER. They then went to the electron beam lithography clean room to view the electron beam patterning process.

The next week, during their lab sections, they observed the etching process. The etching was done using a PlasmaQuest ECR plasma etcher. The plasma composition was CF4:O2 = 15:1 [sccm], at a pressure of 10 mT. The microwave power used to generate plasma was 100 W and an RF source at 50 W was used generate a DC bias voltage of 150 V. The etch rates were determined by etching base silicon samples and measuring the film thickness before and after etching using reflectometry. The etch rate for silicon was determined to be 60 nm/min, and for the resist ZEP520a was determined to be 120 nm/min. This is an underestimate of the actual etch rate since these rates were calibrated using plane chips which have a uniform surface height, whereas it takes more time to etch into the small features of the actual sample. Therefore,

in order to etch the silicon from an initial thickness of 220 nm down to 90 nm, 130 nm of silicon needed to be etched. At an etch rate of 60 nm/min, the required etch time was found to be 130 seconds. After the etching process students used an electron microscope to image their devices.

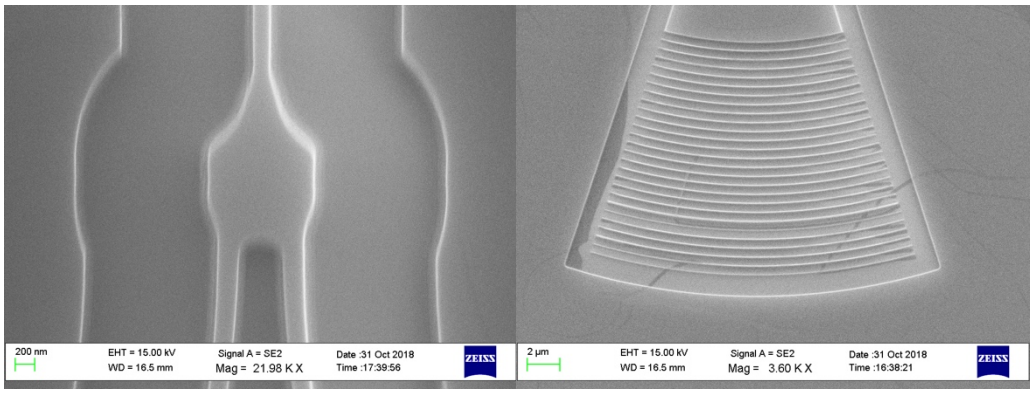

Figure 3. On the left is a y-splitter after the ECR etching process. These are used in the student designs to produce the interferometers used in the thermo-optic switches. On the Right is a grating coupler after the ECR etching process. These are used to couple light into the thermo-optic switches.

After etching, the chips were cleaned in buffered oxide etch (BOE) and then the spin-on dopant, P509 Filmtronics [2] was spun onto the chip. Then the dopant was diffused at 900ºC for 30 minutes to achieve a background sheet resistance of 30 Ω/cm^2. The chip was then cleaned again with BOE to remove any remaining residue.

The next step was to use photolithography to define the N++ dopant regions. Students observed their pattern being loaded into an Intelligent Micro Patterning SF-100 maskless lithography system. The pattern was then exposed. After development, Electron-beam evaporation was used to deposit SiO2 as a diffusion mask. Then lift-off was used to produce the pattern.

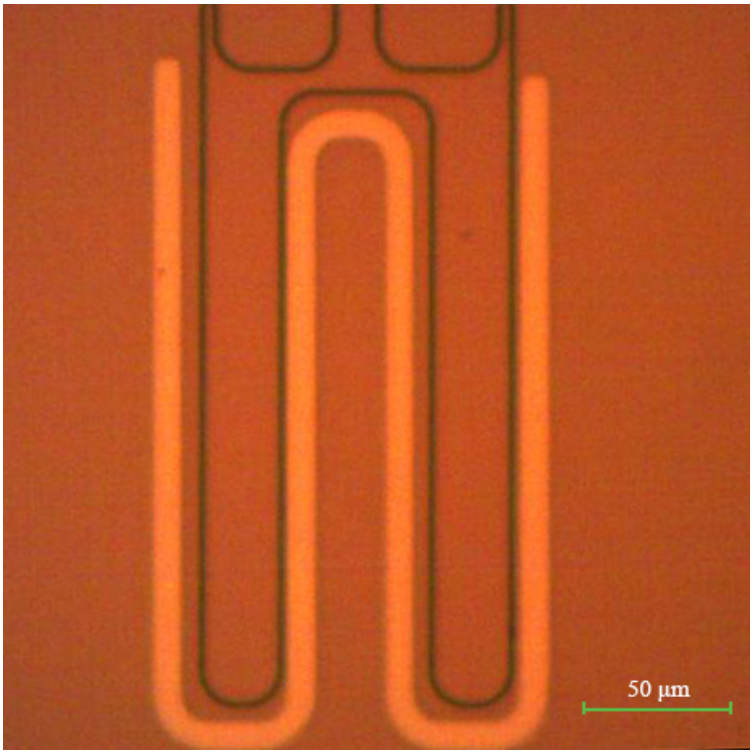

Figure 4. The chip after the oxide lift-off process. The light area is exposed silicon where the N++ dopant will diffuse. The darker area is the oxide mask.

Dopant was then again spun onto the surface. It was diffused at 1100ºC for 30 minutes to achieve a contact sheet resistance of 4 Ω/cm^2. The chip was then cleaned again with BOE to remove any remaining residue.

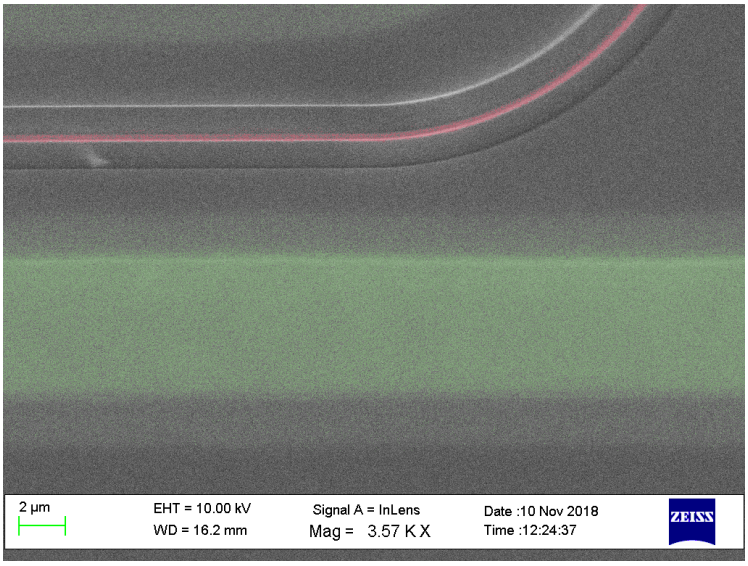

Figure 5. A false-color SEM image of an interferometer with the diffused N++ contact dopant. The N++ contact dopant is visible in green. The 220nm thick silicon waveguide is visible in red. The gray area represents a 90nm thick silicon slab.

The last step in the fabrication process was the deposition of the gold/titanium contact pad. This was done using the maskless photolithography system followed by using E-beam evaporation to deposit a 30 nm titanium layer followed by the 200 nm thick gold contact pads.

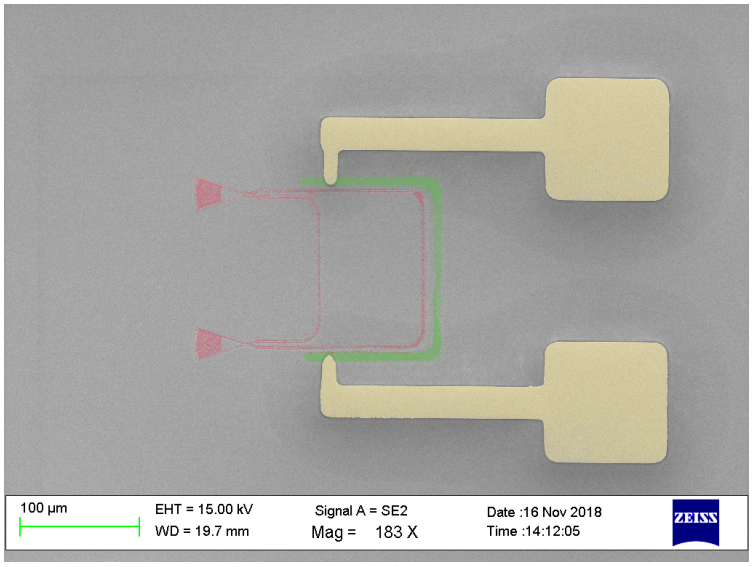

Figure 6. A false-color SEM image of an interferometer with the diffused N++ contact dopant and gold contact pads. The red area represents the silicon waveguides and grating couplers that make up the thermo-optic switch. The green area represents the N++ contact dopant. The gold area represents the gold contact pads.

4. RESULTS

The students used our automatic photonic probe station[1] to measure their devices. After the initial automated optical characterization, the best devices were selected for manual electrical characterization. This was done by using the automatic probe station to position the fiber array over the grating coupler. Then manual electrical probes were used to contact the gold electrical pads. A Keithley 2400 source meter was then used to obtain the IV characteristics.

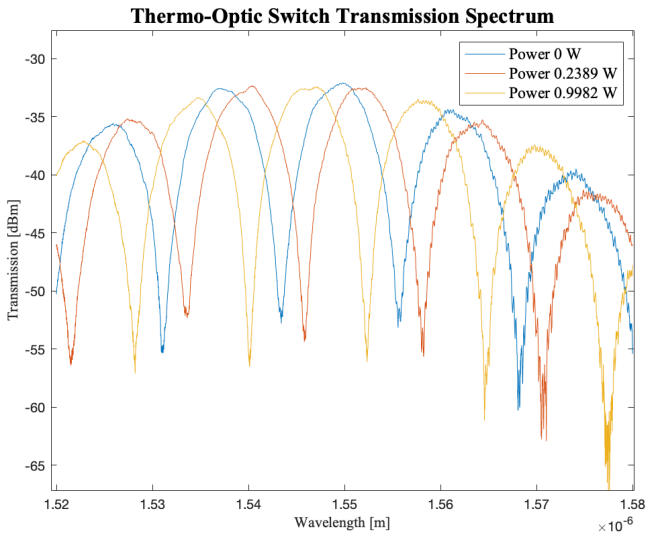

Figure 7. The transmission spectrum of one of the thermo-optic switches. The power consumption is high for a number of reasons. First, this measurement includes the contact pad resistance which is comparable to the heater resistance. The second major element is the 90nm silicon slab dissipates the heat away from the waveguide, wasting power. In the future, this can be easily eliminated by performing a second silicon etch to isolate the heater and waveguide from the remainder of the chip.

The last major class activity was for the students to write a “mock" journal paper, with a goal of teaching students how to collaborate with many people (the entire class) on writing a single document that attains a quality suitable for submission to an academic journal. Each student chose a section that they were interested in writing, and an online platform was used for collaboratively writing the document (Overleaf) [13]. After producing an initial draft, a peer review process was done through the online platform we used (open edX platform) [14] to improve the content. We then held a three hour session where students presented their section using, again, a collaboratively-developed set of slides; this allowed for a round of questions and feedback, including fact-checking by the course’s teaching staff. This process also gave students the important experience of presenting their work outside of their immediate classroom environment. As can be expected, challenges were encountered, including a) too much information and content included in the manuscript; the challenge was keeping the manuscript concise, b) differences in writing style, tone, figure formatting, c) inconsistency between sections on technical details, such as which device was fabricated and which was tested, and what fabrication steps were used, particularly since multiple chips were fabricated and tested.

5. CONCLUSION

Despite the challenges encountered, the course was a success. The students learned the required course content and gained the added benefit of being involved in a research project. The spin-on dopant process shows great promise for the rapid prototyping of silicon photonics. The area where the most improvement to the course could be made is the "mock" journal paper. In the future, we will attempt to encourage more collaboration between the students early on in the course, and help the students develop a set of consistent laboratory notes.

6. ACKNOWLEDGEMENTS

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