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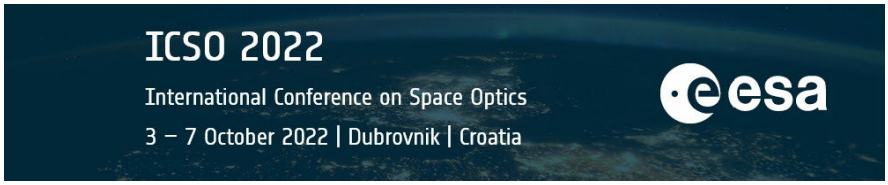

The European Low Fux (CMOS) Image Sensor: a motion artefact free image sensor with High Dynamic Range for space applications.

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The European Low Fux (CMOS) Image Sensor: a motion artefact free image sensor with High Dynamic Range for space applications.

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ABSTRACT

ELFIS2 is the second generation of the European Low Flux Image Sensor (ELFIS), developed by Caeleste, manufactured at LFoundry and tested by Airbus on behalf of the European Space agency.

As the High flux program was aborted, it was decided to continue ELFIS as a High Dynamic Range (HDR) sensor, enabling the simultaneous integration and readout of the same charge packet on a large and a small conversion capacitance. It is combined with charge domain global shutter, so that motion artefacts, typical for multi-exposure or dual photodiode architectures are completely eliminated.

The ELFIS core pixel uses the Global Shutter technology pixel, developed at LFoundry, allowing charge domain Integrate-While-Read operation and on-chip CDS. In order to handle photocharge packets that exceed the full well of the core pixel, there are two low gain overflow capacitors, used alternatingly for signal integration and read-out.

Whereas ELFIS1 was a fixed size device, ELFIS2 is designed for stitching. The stitch block of 512*1024 pixels can realize every n*m multiple of 1/2k by 1k pixels, as long as it fits on the wafer. The Initial prototype presented has a 2k*2k format. 4k*4k, 8k*8K, etc. can be realized with the same mask set, as well as elongated (hyperspectral) sensors up to 512*10 k pixels. As each stitch segment has its own output amplifiers, the ultimate frame rate is only determined by the number of rows to be read. Frame rate can be increased by applying row random addressing, which are especially versatile in hyperspectral applications.

The initial functional tests of ELFIS2 are promising: without further optimization the noise spec of less than 5 e-rms is reached with a HDR full well of 160 ke^-; the core Global Shutter high gain full well is 10 ke^-, resulting in a smooth photon shot noise limited behavior from the high gain noise floor till the low gain saturation.

The full functional testing and circuit optimization is now starting and will be finished at the moment of this presentation. Also, radiation pre-qualification is planned. Due to the good SEE results obtained in another Rad-Hard by Design (RHbD) in the same technology we are also confident that the SEE will have a LET > 63 MeV/mg/cm^2 for both SEL and SEU.

Keywords: CIS, CMOS Image Sensor, Global Shutter, High Dynamic Range, HDR, Rad Hard by Design

1. INTRODUCTION

ESA wants to establish its technological independence of the other continents for critical – mainly dual-use – technologies to be used in the Earth observation and the science missions. CMOS image sensors are considered an important technology to be mastered by European industry. For this purpose, ESA has launched 2 programs to demonstrate the full European capabilities: the European High Flux Image sensor and the European Low Flux Images Sensor or ELFIS [1].

Unfortunately, the first program was aborted pre-maturely. For this reason, it was decided to extent the scope of the ELFIS device to allow multiple gains to cope with a larger dynamic range of signals. Caeleste has decided to introduce High Dynamic Range or HDR readout. In this way: a larger range of missions is in reach of the ELFIS sensor; the ELFIS sensor can cope with a very broad signal range without adjusting the operational parameters (e.g the night- and day-time recording on a sun-synchronous orbit can be made without integration time or gain tuning. For this reason, ELFIS2 is designed as a stitchable image sensor, allowing to make a large staring array and a very elongated hyperspectral sensor with 1 and the same reticle set and by only changing the wafer stepper pattern [2-5].

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2. ARCHITECTURE

ELFIS2 has a slightly modified pixel concept compared to ELFIS1 to allow a higher Charge to Voltage Factor (CVF) in High Gain (HG) mode; the core pixel concept is shown in see Figure 1.

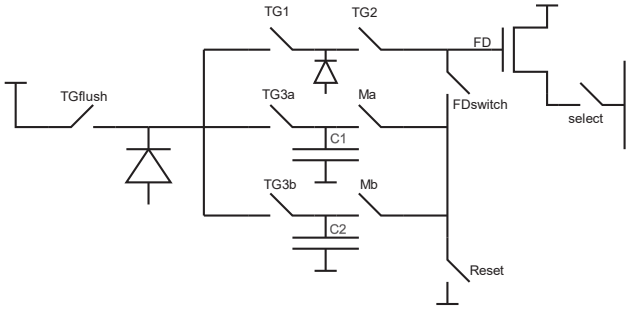
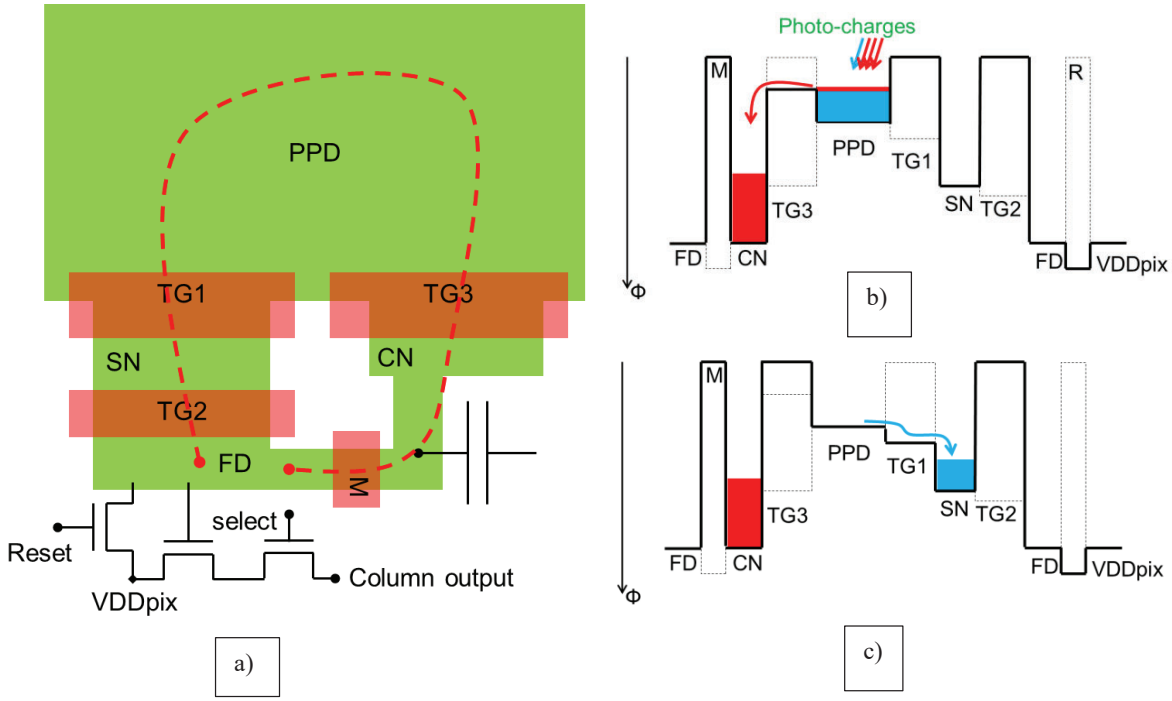


Figure 1: Schematic representation of the new ELFIS2 Pixel. FD isolation is highlighted.

The HDR capability of the ELFIS1 pixel is maintained as indicated in the simplified pixel layout and potential diagram in Figure 2. The pixel allows to simultaneously read out a high gain and a low gain signal from the same photocharge during the same integration time, in a global shutter fashion. The two signals are off-chip combined. In this way motion artefacts, often encountered in other high dynamic range image sensor concepts are eliminated [6-7].



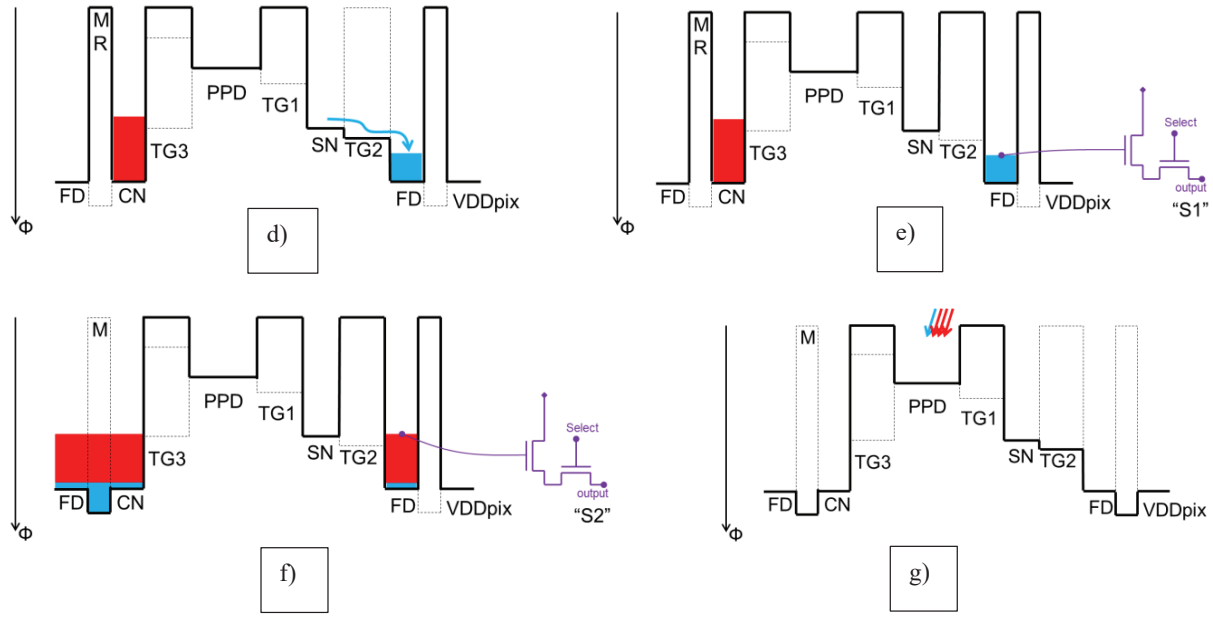


Figure 2: a) Simplified floor plan of the ELFIS pixel with the Contour (red dashed line) for the potential profile discussions - b) to g) potential diagrams during the different phases of the charge accumulation and read-out cycle.

in Figure 2 a), the simplified pixel layout and the contour for the potential profile discussion is shown. Figure 2 depicts the potential diagrams and the charge build-up during the integration time: the charges, generated for a faint signal, are retained within the photodiode (PPD) while the charges, generated for a large signal, are completely filling the PPD and overflowing via Transfer Gate3 (TG3) into the Capacitor node (CN). At the end of the integration time, the signal contained in the PPD is transferred via TG1 into the Intermediate Storage Node (SN) (see in Figure 2 c)). When a line is read out the Signal charges of SN are transferred to the Floating Diffusion (FD) node for Charge to Voltage conversion (in Figure 2 d and e); The circuit also allows to execute Correlated Double sampling (CDS) by reading out the reset level in the line time prior to the signal readout. After the high gain read-out the Merge Transistor (MR) is opened and the low-gain signal is read out through the same Source Follower transistor (in Figure 2 f). Finally, the CN capacitor is reset via the MR transistor and the FD node (in Figure 2 g); while in the meantime the next integration cycle is already started in the PPD node [2,4,5].

The pixel pitch (15 µm) of ELFIS1 is maintained. The charge storage is further optimized to reach approximately 10 ke- full well in high gain, by tuning the implant conditions for the intermediate storage node; The Low Gain charge storage capacity is maintained at 160 ke- in IWR mode and 320 ke- in ITR mode.

Figure 3 shows the ELFIS2 stitching configuration[5].

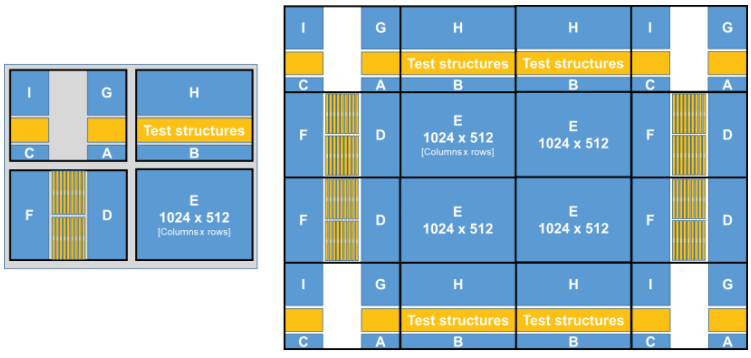


Figure 3: Left: Reticle design with the 4 stitch blocks- Right: stitched configuration for a 2k*1k design.

The first realization of ELFIS2 is a 2k*2k imager consisting of 2*4 stitch blocks.

The analog signal chain (see Figure 4) remained more or less unchanged since ELFIS1 apart from punctual optimizations.

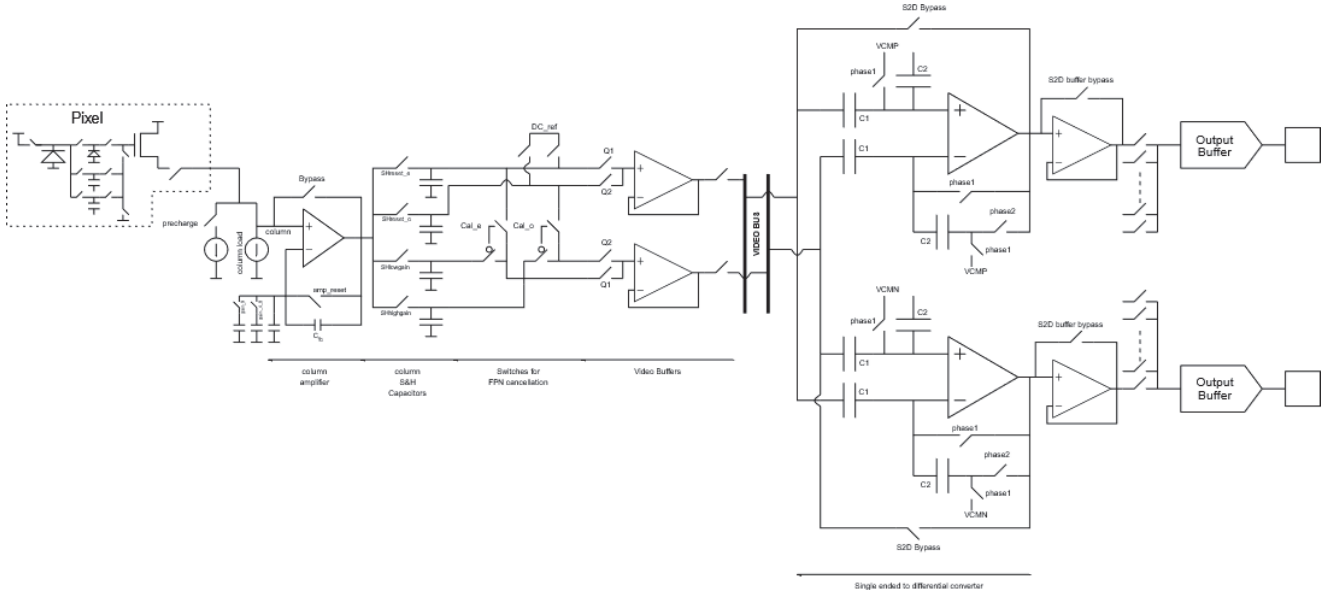


Figure 4: Analog chain of the ELFIS2 signal flow from pixel to analog output buffer.

Additional features as compared to ELFIS1.

Three additional features are included in the device [3]:

1) Demonstration of 2x2 pixel charge domain binning
2) Design precautions to allow back-biasing to achieve full depletion when using a high resistivity substrate or epi layer.
3) The use of thick epi-layers with a final thickness of [22 – 24 µm] to achieve a better NIR responsivity.
The features 2) and 3) are designed in close collaboration with the foundry where the doping profiles are optimized with TCAD simulations.

3. INITIAL RESULTS

The processing of the ELFIS2 devices is set up as a design of Experiments. A part of the wafers is processed with thin epi material and the same implant conditions as for the best wafers of the ELFIS1 campaign. A second group of wafers is processed with a 12 µm thick epi layer. 1 subpart with an identical process as the thin-epi wafers and another part with special features to apply back-bias and full depletion of the epi layer. A last part of the wafer lot is processed with a 22 µm epi layer, also including the features for deep depletion.

Table 1: Lot split options for the first ELFIS2 prototyping lot

Group	#wfrs	Stitch config	BSI/FSI	DEEP NWELL	p+ implant on backside	starting material	Final Thickness
A1	2	2k*2k	FSI	no	no	EPI 6um LowRES	4um
A2	2	2k*2k	BSI	no	no	EPI 6um LowRES	4um
A3	2	2k*2k	BSI	no	no	EPI 14um HiRES	12um
A4	2	2k*2k	BSI	YES	YES	EPI 14um HiRES	12um
A5	2	2k*2k	BSI	YES	YES	EPI 14um HiRES	12um
A6	2	2k*2k	BSI	YES	YES	EPI 24um HiRES	22um

Initial ELFIS2 devices are assembled on a small PCB as Chip-on-Board (CoB). The device is protected with a BroadBand Anti-Reflective (BBAR)coated protective glass (see Figure 5-Left). Not visible on the photo is the heat slug attached to the PCB for efficient cooling of the device. In parallel the ceramic package for the in-depth validation is designed and produced as well and are waiting now final assembly of the devices for functional testing (see Figure 5-Right). The pads on the top rim of the package are for assembly of auxiliary decoupling capacitors; the package contains a recess for the window lay-up.

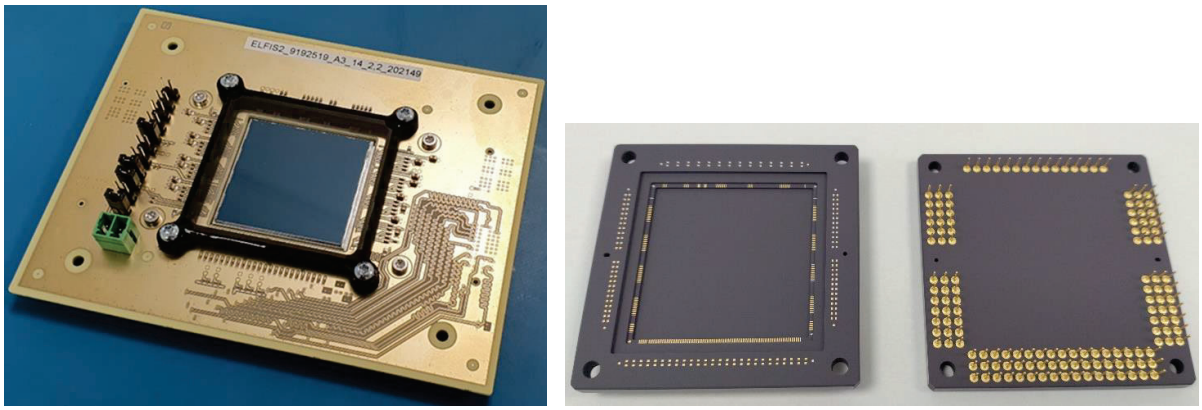


Figure 5: Left: Present CoB assembly of the first ELFIS2 devices - Right: package for the future flight devices

The first devices are assembled blindly, as the probe card and the probing routines are not yet in place. Most assembled devices are functional with cosmetic defects. Figure 6 show the first images of an EIA-1956 test chart in full resolution (2k*2k pixels) and of an image with a vertical Window of Interest (WOI) applied (2k horizontal and 1k pixels between rows 512 and 1536 vertically). Some line defects are visible in the images. The images are taken in Global Shutter High gain mode with on-chip CDS and externally applied dark signal correction.

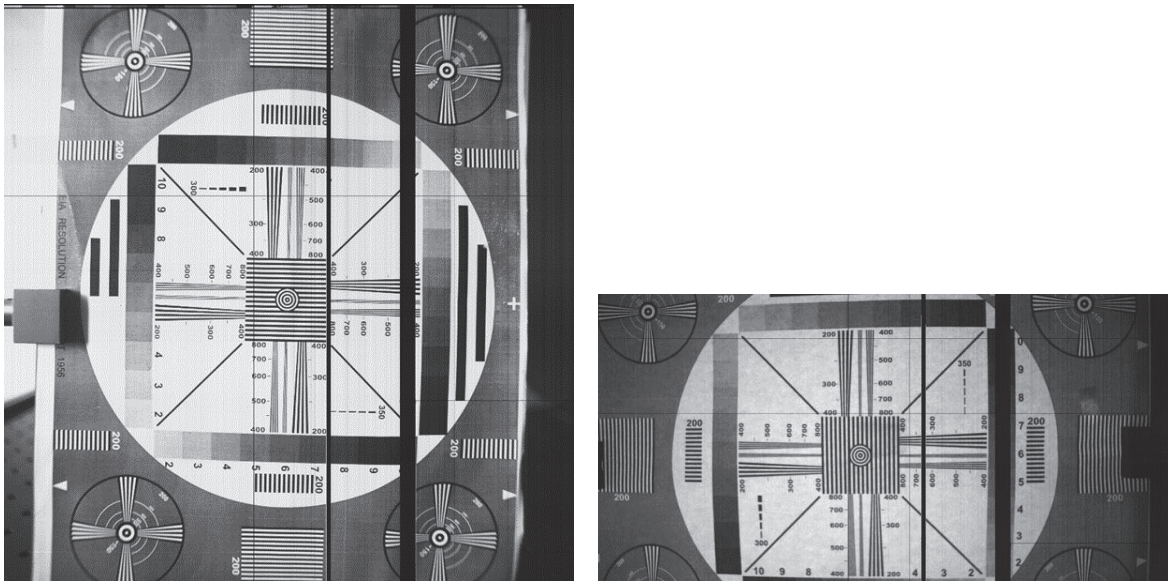


Figure 6: Image of an EIA-1956 test chart in full resolution (Left) and an image with a vertical ROI between rows 512 and 1536. (Right)

As the thick epi was a new development, an initial test on the spectral response was also performed. The influence of the epi-layer thickness on the NIR quantum efficiency is clearly visible (Figure 7). The graph refers to the nominal epi layer thickness before back-etching and backside polishing; the effective thicknesses are 12, respectively 22 µm. Further optimization of the ARC thickness is still planned. In principle, such devices can have a QE_{peak} of ≥ 95%.

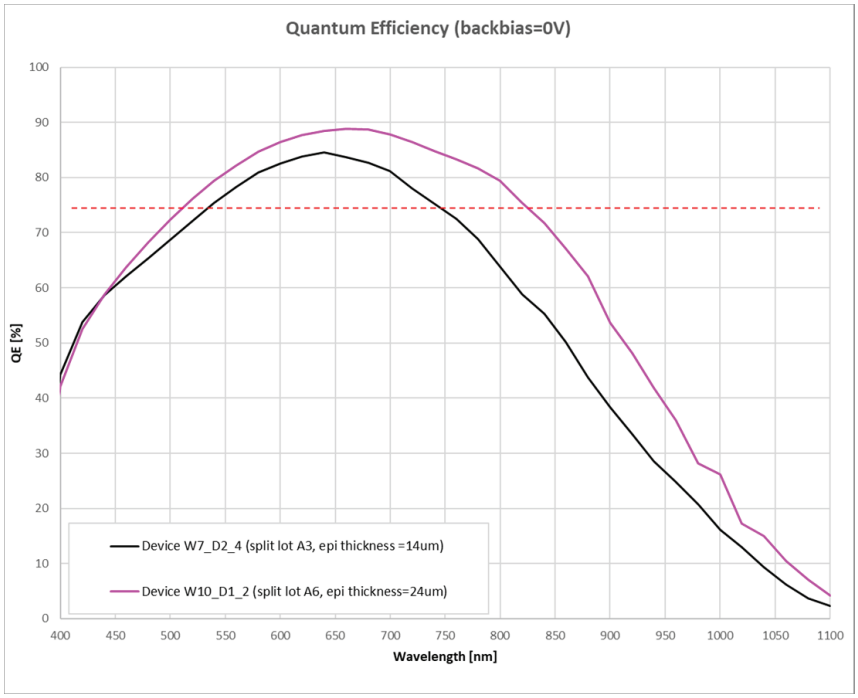


Figure 7: Spectral response measurement of an ELFIS2 sensor with an epi thickness of 12, respectively 22 µm.

The most important electro-optical parameters are summarized in Table 2. It is immediately visible that the main objectives of the redesign are achieved: The full well of the High Gain mode is better matched with the Low Gain signal vs noise curve to avoid jumps in noise performance, when switch gain ranges. The read noise is almost halved w.r.t. to the detailed ELFIS1 measurements. The dark current is higher than for ELFIS1, this was anticipated as the depletion volume is considerably larger and the dark current for this type of devices is mainly driven by the bulk G-R phenomena. The output amplifier power is also in line with the expected and previous results. All the other electro-optical properties (image lag, Parasitic Light Sensitivity, MTF, …) will be verified after the optimization of the operational conditions.

Table 2: Summary of most important Electro-optical parameters during the CoB pre-characterization phase.

	Test name	ELFIS2 Result		Spec	ELFIS Result
Pre-characterization	CVF & FW	**114µv/e- and 11ke-**		10ke-	6ke-
	read noise	**4.6e-**		<5 e-	8.7e-
	Dark current	*14µm @35°C:*	*24µm@35°C:*	<50pA/cm²	9 pA/cm² on thin epi
		36.9pA/cm²	48.9pA/cm²		
	Power	22mW per channel		50mW per channel	26 – 40 mW

4. PLANNED ACTIVITIES

The assembly of the first devices in ceramic package is planned for Q4/2022 or Q1/2023; In the meantime, devices are assembled as CoB for validation. Once these devices will be received at Caeleste, the operation of the ELFIS2 devices will be further fine-tuned for the operating modes, agreed with the Agency. It is expected that the room temperature tests (first row in Table 3) will last until the end of September 2022. Then there is time foreseen for TID and SEE testing. As Caeleste finished the heavy ion test campaign on another device in the same technology and with the same design methodology, we expect to reach a LET value > 63 MeV/mg/cm^2.

Table 3: Planned test campaign on the ELFIS2 2k*2k version

Electro-Optical test summary.

Condition	Temp.	QE	PLS	MTF Xtalk	Defects	Idark	Noise	Response	PRNU	Image lag
		12b	27	15/16	24	17-18	13-14-25	21-22-23	23	26
GS HG on-chip CDS	293-233K									
	203K									
	173K									
RS LG on-chip CDS	293K									
	173K									

Specification measured before and after the irradiation tests

Condition	Temp.	QE	PLS	MTF Xtalk	Defects	Idark	Noise	Response	PRNU	Image lag
		12b	27	15/16	24	17-18	13-14-25	21-22-23	23	26
GS HG on-chip CDS	ambient									
RS LG on-chip CDS	ambient									

As a last part of the validation campaign the low temperature behavior of the devices is planned for the November-December time frame. Finally, also a test in thermal vacuum chamber at low temperatures ADS in Toulouse is planned of the first quarter of 2023. But in view of the present positive results, Caeleste is in a position to discuss upcoming projects, based on the present device architectures. It shall be noted that mainly the elongated versions of the ELFIS2 with (2k – 8k) * 512 pixels with 560 full frames per second are very interesting candidate image sensors for hyperspectral applications. When a vertical ROI of 256 rows is applied, a kHz frame rate is in reach.

5. CONCLUSIONS

The redesign of the ELFIS sensors was concluded and the initial measurements show that the results are in line with the expectations. The noise of the image sensor is further reduced to 4.5 e^-_{rms}; the dark current is in line with the expectations for a thick epi layer. Also, the additional features to allow back-biasing are working well. The manufacture with thick epi layers to increase the NIR response has proven to be successful. The performance for charge domain 2*2 binning needs further analysis and will be reported later.

ELFIS2 is also a stitched design based on 1024*512 pixels basic stitch block. The first demonstrator device is the 2k*2k version, but all formats ranging from 1k*0,5k till 8k*8k are in reach. Also, very elongated devices, suitable for hyperspectral imaging and with full frame rates of 560 fps are in reach.

The initial testing of the ELFIS2 as CoB is finished and the validation devices are under assembly. These devices will be subjected to full room temperature characterization to further optimize the operational conditions. Low temperature testing, low temperature thermal vacuum chamber testing and radiation testing are also planned.

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