On the integration of memristors with CMOS using nanoimprint lithography

Qiangfei Xia [a], W. M. Tong [a, b], W. Wu [a], J. J. Yang [a], X. Li [a], W. Robinett [a], T. Cardinali [b], M. Cumbie [b], J. E. Ellenson [b], P. Kuekes [a] and R. S. Williams [a]

[a] Information & Quantum Systems Lab (IQSL), Hewlett-Packard Laboratories, 1501 Page Mill Rd, Palo Alto, CA 94304
[b] Technology Development Operations (TDO), Hewlett-Packard Company, 1000 NE Circle Blvd., Corvallis, OR 97330

E-mail: qiangfei.xia@hp.com

ABSTRACT

Memristors were vertically integrated with CMOS circuits using nanoimprint lithography (NIL), making a transistor/memeristor hybrid circuit. Several planarization technologies were developed for the CMOS substrates to meet the surface planarity requirement for NIL. Accordingly, different integration schemes were developed and optimized. UV-curable NIL (UV-NIL) using a double layer spin-on resists was carried out to pattern the electrodes for memristors. This is the first demonstration of NIL on active CMOS substrates that are fabricated in a CMOS fab. Our work demonstrates that NIL is compatible with commercial IC fabrication process. It was also demonstrated that the memristors are integratable with traditional CMOS to make hybrid circuits without changing the current infrastructure in IC industry.

Keywords: Nanoimprint lithography, memristor, CMOS, transistor, integration, planarization

1. INTRODUCTION

Semiconductor nanowires interconnect (SNIC) is a hybrid architecture of nanowire crossbar/CMOS which has several advantages over conventional transistor-based field-programmable gate arrays (FPGA) in terms of density, functionality and power consumption [1, 2]. In SNIC, the data routing network is separated from the Si CMOS layer using field programmable nanowire crossbar arrays. Because the routing layer is placed directly above the CMOS circuit, the chip footage area is smaller, and the talking distance between the transistors are shorter, leading to smaller chip size and higher processing speed. Moreover, the cross bar structure ensures that defects can be routed around, resulting in a very highly defect-tolerant circuit.

In SNIC, the data routing network consists of metal nanowires and memristors. Memristors (short for memory resistor), postulated in 1971 and "found" in 2008 [3, 4], are two-terminal passive devices which are considered the fourth basic element of an electrical circuit. One implementation of a memristor in a vertical configuration is using two metal electrodes with a switching material layer sandwiched in between. The switching material is usually a transition metal oxide: for example, TiO_x. One possible working mechanism of a memristor of this type is related to the oxygen vacancy movement under an applied electrical field [5]. As a result, memristors exhibit non-linear electrical behavior. The key advantage of memristors over other memory technologies of today (e.g. flash) is that it a memristor cell can be very compact (< 10 nm), and as we demonstrate here, be integratable with today's CMOS technology.

Alternative Lithographic Technologies, edited by Frank M. Schellenberg, Bruno M. La Fontaine
Proc. of SPIE Vol. 7271, 727106 · © 2009 SPIE · CCC code: 0277-786X/09/$18 · doi: 10.1117/12.814327

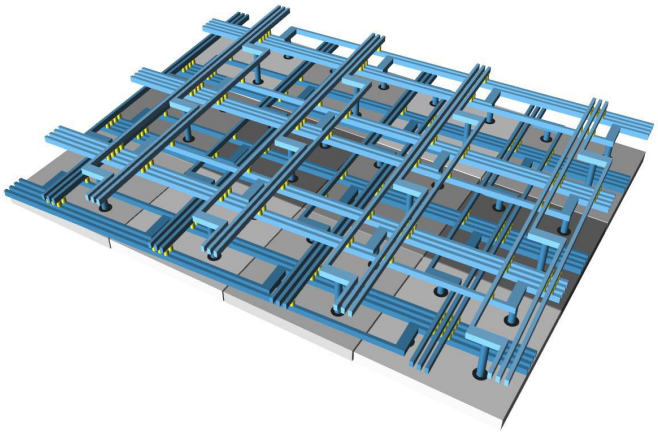

Figure 1: Schematic of the memristor-transistor hybrid chip in which the memristors are the configurable wiring used for wiring up the transistors to make a digital circuit. The gray substrate is the CMOS layer. The switching material (yellow) and pairs of blue wires form memristors that are connected to the CMOS through the vias. (Courtesy, Greg Snider, HP Labs).

In this paper, we report the implementation of the memristor/transistor hybrid circuits by vertical integration of memoristors with CMOS circuits using nanoimprint lithography (NIL). The memristors are integrated with transistors in the CMOS layer in a 3-dimensional (3D) fashion. With this memristor layer as data routing network, we achieved a new type of FPGA-like architecture. This is the first demonstration of NIL on active CMOS circuits that are fabricated in CMOS fab. Successful integration indicates that the hybrid circuits can be realized using NIL without changing the infrastructure of the IC industry, and opens up more application opportunities for memristors in other fields.

In the following sections, issues and solutions in the integration process are discussed. The integration principle is first introduced, followed by the details of NIL process. In particular, we focus on several planarization approaches.

2. INTEGRATION WITH NANOIMPRINT LITHOGRAPHY

2.1 Integration principle

The integration started with CMOS substrates that were fabricated in HP CMOS fab located in Corvallis, OR. We deliberately employed a trailing-edge 0.35 μm process to demonstrate the utility of the SNIC architecture and to uncover any potential integration issues with nanoimprint. On the CMOS substrates, tungsten (W) vias were designed for the contact between the CMOS and the metal nanowires. These W vias, one set (shown in red in Fig. 2a) for the bottom electrodes and the other set (shown in blue in Fig. 2a) for the top electrodes of memristor were exposed after chemical mechanical polishing (CMP) of the TEOS layer on top of the CMOS chip.

NIL was used for patterning both the bottom and top electrode nanowires. In order to cover the W vias on the CMOS substrate, large pads were designed and fabricated with the nanowires. Each pad has two nanowires stretching out, with a small angle rotation so that each nanowire is going to connect to only one W via.

For the memristor crossbars fabrication, the bottom electrodes were first patterned on the CMOS substrate using UV-NIL, followed by reactive ion etching (RIE) and metallization (Fig. 2b). Second, a thin layer of TiO_x (about 30-40 nm) was deposited as the switching material either by sputtering or by atomic layer deposition (ALD) (Fig. 2c). Third, the top electrodes were fabricated on the switching layer in a similar manner as for the bottom electrodes (Fig. 2d). Finally, contacts between the nanowires and the W

vias on the CMOS chip were made by photolithography and metal deposition (Fig. 2e, 2f). It has to be pointed out that the approach aforementioned is only one of the schemes for the integration, variants are described in this manuscript later on.

The detailed fabrication of the electrodes using NIL is schematically illustrated in Fig. 3. We used double layer resists, one as imaging layer and the other as transfer layer; both were spin-coated on the substrates [6]. After UV-NIL using a quartz mold, the residual imaging layer and the transfer layer were etched using RIE processes with different gas chemistry. Undercuts were intentionally made in the transfer layer for the ease of liftoff of the metals, which were deposited using an electron beam evaporator.

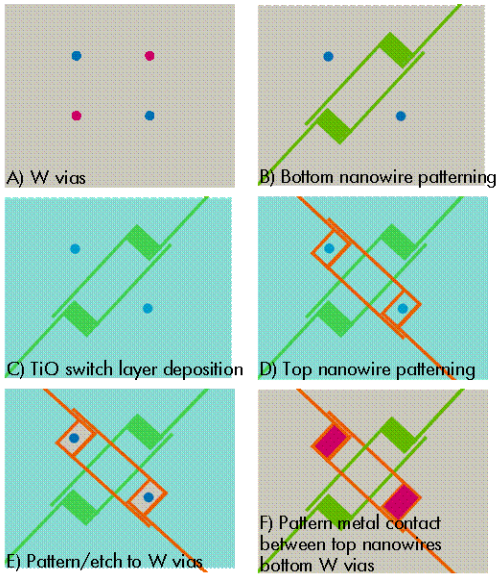

Figure 2: Schematic of one integration scheme. (A) Two sets of W vias were exposed on the CMOS substrates (B) NIL was used to pattern the bottom electrode. (C) Deposition of switching layer. (D) Top electrode patterning using NIL. (E) and (F) One approach of making contact of the top electrodes to the other set of W vias .

2.2 NIL molds fabrication

To make the molds used for patterning the bottom and top electrodes, electron beam lithography (EBL) was carried out to pattern the 100 nm half-pitch features and the grid structured contact pads on Si substrates covered with 50 nm thick thermal SiO_2. The SiO_2 was etched to 50 nm deep by RIE. After being treated with an anti-adhesion layer in a custom made tool, the master molds were used to duplicate daughter molds in quartz by NIL and RIE. Quartz was chosen as the daughter-mold substrate material because it is transparent to the UV light used in the NIL process. The quartz molds were treated with an anti-adhesion layer before being used for NIL. Optical microscope images and an AFM image of the grid structured contact pad are shown in Fig. 4. It is worth noting that the pad was designed as a grid structure instead of a solid one. This design has the following two advantages. First, the residual layer will be more uniform after NIL because the grid structure will improve the resist flow. Second, the openings in the grid will allow for RIE of the material underneath as necessary for the process described in Fig. 2.

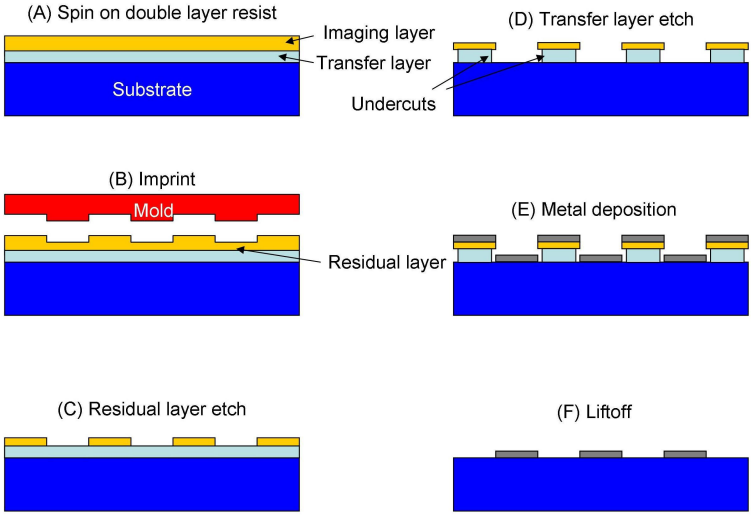

Figure 3: Schematic fabrication process for the electrodes. (A) Spin on double layer resists. The imaging layer is UV-curable. (B) UV-NIL process. (C) RIE of the residual layer. (D) RIE of the transfer layer. An over etch is carried out to make a proper undercut. (E) Metal deposition using an e-beam evaporator. (F) Liftoff in acetone.

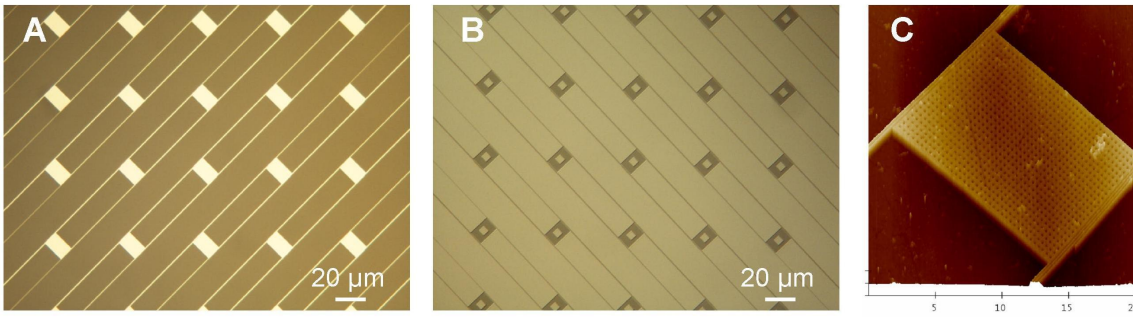

Figure 4: Optical microscope and AFM images of the molds. (A) Mold for top electrode. (B) Mold for top electrode. The lines in (A) and (B) are groups of nanowires with 100 nm half-pitch. The pads are 10 um by 15 um. The squares in the pad centers of (B) are designed for RIE of switching materials underneath (see Fig. 2E) and they are 5 um by 5 um in size. The pads are composed of grids with a pitch of 400 nm (C).

3. PLANARIZATION OF THE CMOS SUBSTRATES

Although the CMOS substrates have been polished using CMP after depositing TEOS, the surface flatness may not be good enough for NIL due to the dishing effect in CMP. Surface metrology study showed that W was removed faster than the TEOS, resulting in a surface with the top of W vias lower than the TEOS surface. Issues such as this are expected because the CMOS parts were fabricated with 0.35 µm process. We found that the non-flatness of the as-received CMOS substrates was 40 to 150 nm, depending on the CMP process. Fig. 5 shows a typical image of the CMOS substrate surface morphology with a peak to valley roughness of about 50 nm. We attempted increase the thickness and the polish time of the CMOS top dielectric layer, but at the end we found that the spatial wavelength and size of these features would require

re-lapping of the substrates on a hard surface. This option was not feasible. With this degree of nonflatness, NIL was not successfully achieved on substrates.

After a few unsuccessful attempts to re-CMP the CMOS substrate to reduce non-flatness, we decided that the correct approach is to carry out an extra planarization step before nanoimprint. Several planarization methods have been explored, as discussed in the following sections.

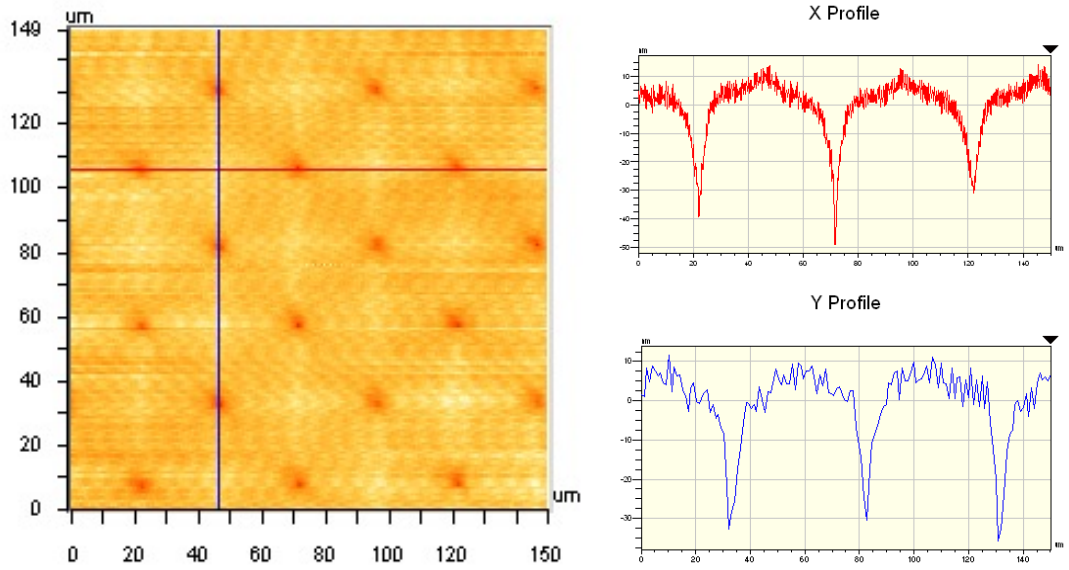

Figure 5: Surface metrology data for the as-received CMOS substrates which were polished by CMP. The red and blue curves are the cross sectional profiles along the red and blue lines in the morphology image, respectively.

3.1 Planarization using the transfer layer material

Using a thermoplastic polymer to planarize a non-flat surface has been demonstrated for other applications such as for phase change memory [7]. In UV nanoimprint, the resist is typical made of a bilayer of the *imaging* layer (UV curable resist) and the *transfer* layer. Using the transfer layer as the planarization layeris appealing because it is a thermoplastic material and it eliminates one process step. Ideally, when the surface is planarized, UV resist can be directly applied on top for NIL.

To planarize using the transfer layer, a thin thermoplastic film was spin-coated on the CMOS substrate. Fig. 6a shows the cross sectional profile of the surface after about 80 nm thick transfer material was spin-coated. The surface non-planarity did change as the polymer follows the CMOS substrate profile. After baking on a hot plate at 90 ^{o}C for 15 min to drive out the residual solvent, the surface quality was not improved (Fig. 6b). One attempt was to reflow the resist at a higher temperature (200 ^{o}C) for a longer period of time (30 min to 120 min). The surface profile improved a little, but it was still not flat enough for NIL even after reflow for 120 min (Fig. 6c).

To effectively planarize the thermoplastic transfer layer, a blank quartz plate was put on top of the substrate with 300 psi external pressure. The quartz plate and the substrate were heated together to 200 ^{o}C for 30 min during which the transfer material reflowed under the pressure to make a flat surface. The surface profile of the substrate after the pressure assisted planarization is shown in Fig. 6d. The non-planarity has been reduced from above 40 nm to below 10 nm.

Successful NIL on the pressure assisted planrizated surface was achieved. With UV resist spin coated on the planarized substrates, NIL was carried out. After etching the residual UV-resist and then the

transfer material (with sufficient over etch), 9 nm thick Pt (with 2 nm Ti adhesion layer) was deposited using an e-beam evaporator, followed by a liftoff process in acetone. The metal nanowires were continuous. The contact pads were sitting directly on top of the W vias, but even so the zoom in image of the pad area showedthe contact with the W vias may not be good because the pads are discontinuous (Fig. 7). Thus the drawback to this approach is that it will impose connectivity problem in the hybrid circuits.

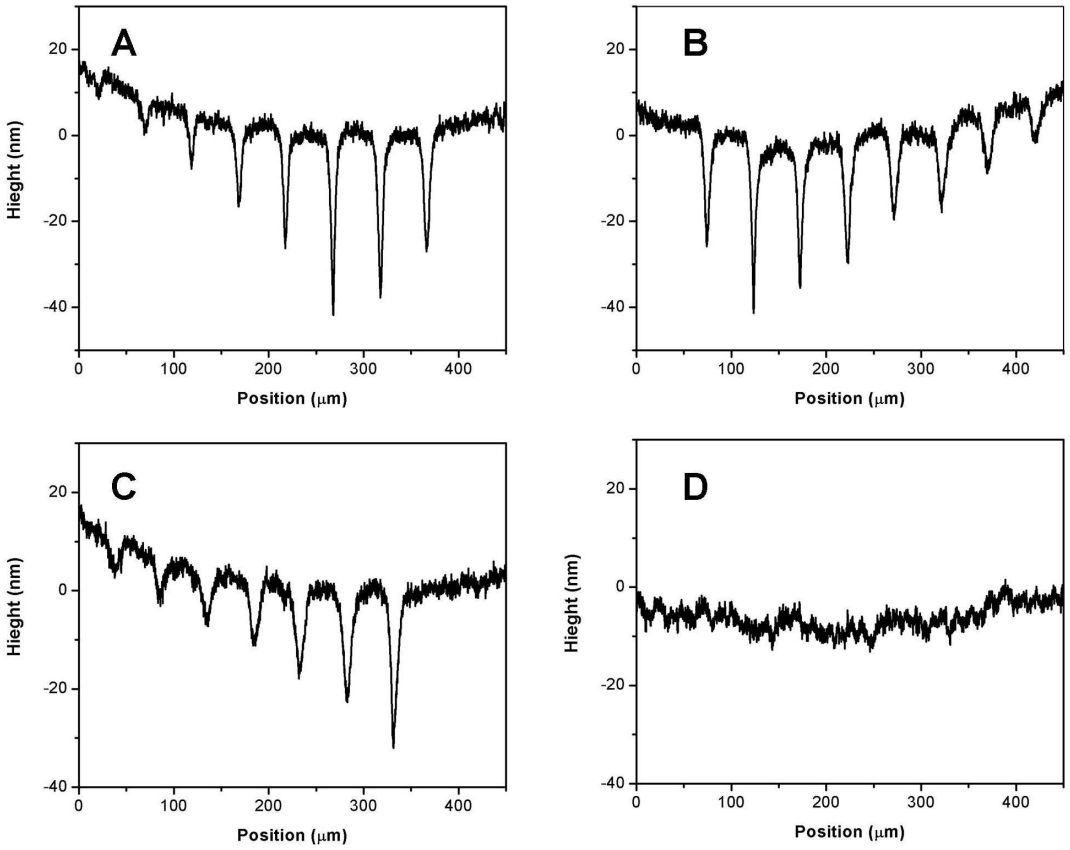

Figure 6: Cross sectional surface profiles for (A) the CMOS substrate after CMP and spin coating of a thin layer of transfer material, (B) the surface after a soft bake at 90 ^{o}C for 15 min, (C) after reflow at 200 ^{o}C for 30 min (there is little change even with 120 min reflow) and (D) after pressure-assisted reflow at 200 ^{o}C under a pressure of 300 psi for 30 min. The surface was planarized to within 10 nm in (D).

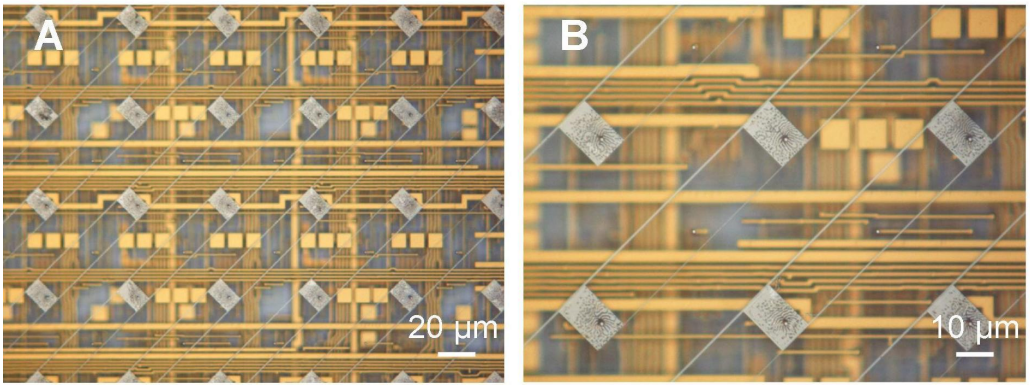

Figure 7: (A) Bottom electrodes patterned by NIL and liftoff on the CMOS substrate that was planarized by pressure-assisted reflow of the transfer layer. The zoom in image (B) exhibits a discontinuous pattern in the pad area, indicating poor connectivity between the bottom electrode and the W vias.

3.2 Planarization using the UV resist

In this approach, an extra layer of liquid UV resist was used as the planarization layer. The UV resist (same as the one used as the imaging layer in NIL) was first spun on the CMOS substrates, followed by a UV-NIL process with a blank quartz plate to flatten the surface. The process was finished at room temperature. Because the planarization material was in its liquid state before UV-crosslinking, it flowed better and a lower pressure was needed than that for a transfer layer material as discussed in section 3.1.

Two sets of substrates, one with 150 nm and the other with 50 nm of as-received non-flatness, were planarized using this approach. As shown in Fig. 8, with 100 and 65 nm thick UV resist, the surface non-planarity was improved from 150 to 20 nm, and 50 to 8 nm, respectively.

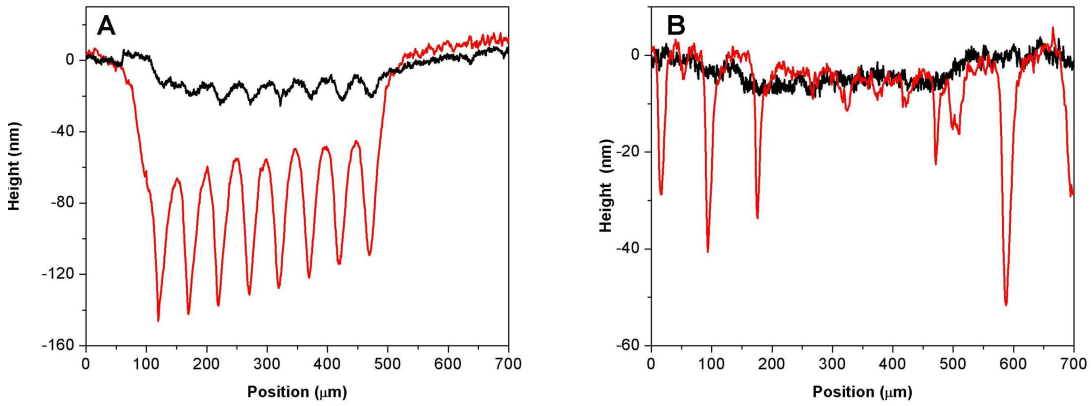

Figure 8: UV-resist planarization. Left: with 100 nm thick UV resist, the 150 nm non-planarity was reduced to 20 nm. Right: 50 nm non-planarity was reduced to 8 nm using a 65 nm thick UV resist. The pressure used for the planarization was 75 psi.

After the planarization, a UV-NIL process was carried out successfully on this cross-linked UV-resist covered substrate. The metal deposition and liftoff were also successful (Fig. 9a). The optical micrograph of the pad areas shows that they are uniform (Fig. 9b). After depositing 40 nm TiOx layer (Fig. 9c), the top electrodes were fabricated with the same fashion (Fig. 9d). The SEM images for some of the finished memristor arrays are shown in Fig. 10.

However, with this planarization scheme, the memristor crossbar layer was electrically isolated from the CMOS layer by the cross-linked UV resist. To connect these two layers, a photolithography step

was conducted to open contact holes in the grid-structured pad area. An RIE process etched the UV planarization layer through the metal grids in the pad areas all the way down to the W vias in the CMOS. A 100 nm thick Pt thin film (with 10 nm Ti adhesion layer) was deposited in the pad area to make connection between the CMOS and the memristor layers, followed by a liftoff process.

One potential issue with this approach is that the final RIE may erode the metal in the grid-structured pads. Although other metals (e.g., Cr) that withstand the plasma during RIE has been chosen to replace Ti as the adhesion layer for Pt [8], the switching properties might be different. Also, the bombardment of the metal by the ionized particles may introduce some adverse effect to the device performance.

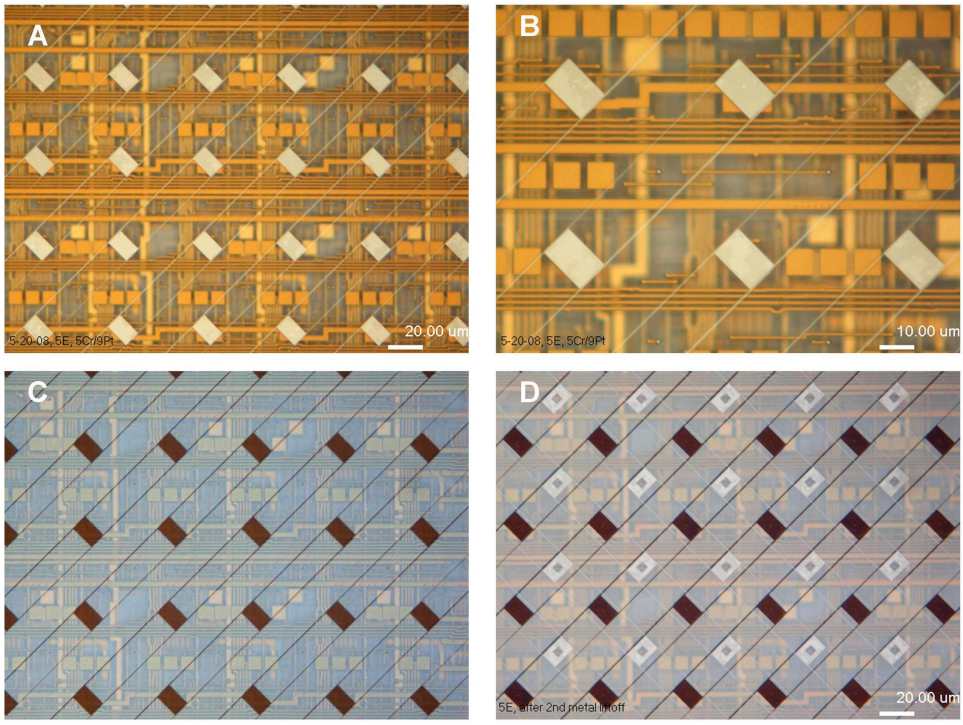

Figure 9: Fabrication of memristor arrays on the UV resist planarized CMOS substrate. (A) Bottom electrode after liftoff, (B) zoom in image of (A) showing uniform pad area. (C) 40 nm thick TIOx was sputter coated on the suface. (D) Memristors were finished afterh the top electrode liftoff. At each cross point of the brown and silver wires there is an array of memrisotrs.

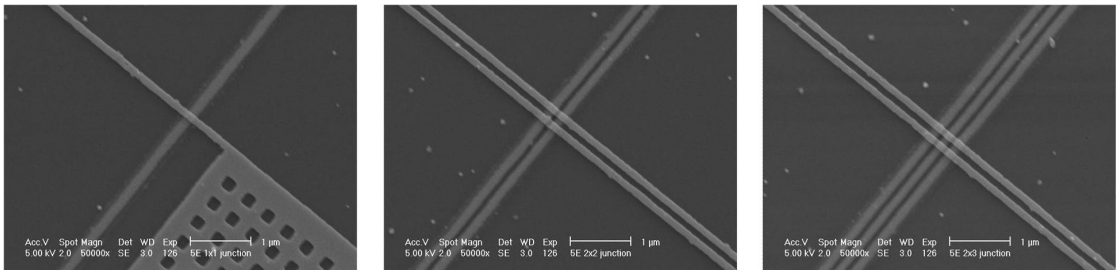

Figure 10: Scanning electron microscope image of the fabricated memristor arrays with the insets show the 1 × 1, 2 × 2 and 2 × 3 arrays. Other array configurations include 1 × 2, 1 × 3 and 3 × 3 (not shown here).

3.3 Planarization by metal back filling

To avoid exposing the contact pads to the RIE process, a modified approach based on UV-resist planarization was proposed, as illustrated in Fig. 11. First, the CMOS substrate was planarized using the UV resist, as described in section 3.2. A conventional photolithography step and a RIE step were carried out to open holes in the planarization layer to expose the top surface of the W vias. Metal plugs (e.g., Ti/Pt double layers) were then deposited on top of the exposed W vias to the level of the TEOS surface by controlling the thickness during evaporation. After liftoff in acetone, the surface is flat enough for the first NIL, during which the contact pads of the bottom electrodes (wires) will be in directly contact with the back-filled metal plugs. As a result, an electrical connectivity was made between the bottom electrode and CMOS through the W vias and the extended metal plugs. The switching material (e.g., TiOx) was then deposited on the whole substrate. With the similar fashion, holes were open and metals were backfilled to extend the other set of W vias (blue), making a flat surface ready for the 2nd NIL which patterned the top electrodes on the switching material surface.

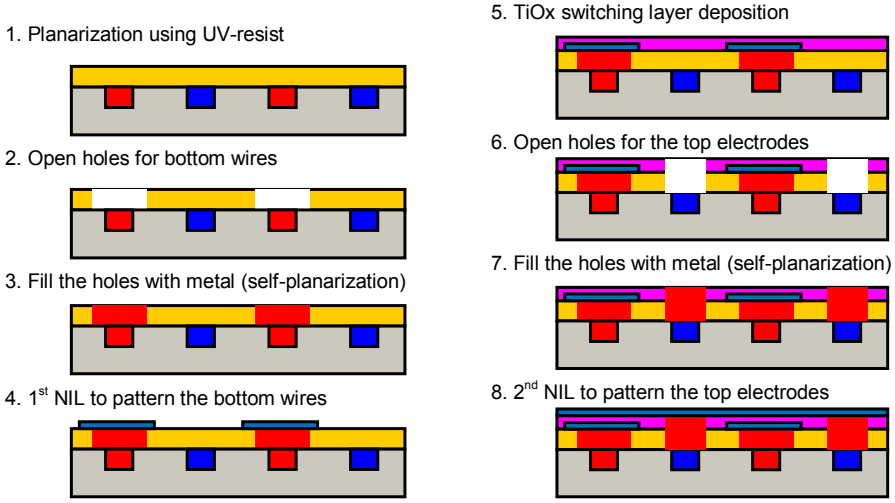

Figure 11: Extending W vias by metal back filling. A UV resist planarization is first performed on the CMOS substrate (1). The red vias in the CMOS layer are then exposed by photolithography and RIE (2), followed by metal back filling to the level of the TEOS surface (3). On the planarized surface, NIL is carried out to make the bottom electrodes (4) which are electrically contacted with the W vias in CMOS. After the switching material is deposited (5), similar processes are conducted (6, 7), and the top electrodes are fabricated by NIL to make contact with the other set of W vias..

For the CMOS substrates with 40 nm non-planarity, a 63 nm thick UV resist was used for UV planarization. After photolithography and RIE to open one set of the W vias (red), 90 nm Pt/10 nm Ti were deposited to fill the wholes to the level of the original TEOS surface. The opening size for each W via was 6 μm by 9 μm so that they could be covered by the pads in the nanowire layer. We used a reversal tone photolithography scheme using AZ 5214E resist, which automatically left a negative slope in the resist after development (resist opening at the surface was narrower than at the root). As a result, there were no liftoff defects such as "rabbit ears", ensuring a flat enough surface for the NIL process for the bottom electrodes. After depositing 9 nm Pt/2 nm Ti as the bottom electrode, and a liftoff in acetone, a 36 nm thick TiOx was sputtered onto the surface. With the similar fashion, the other set of W vias (blue) were extended to the surface of the TiOx film, and the second NIL was performed to make the top electrodes (12 nm thick Pt). Optical microscope images of the chip at different stages are shown in Fig. 12, in which only the bottom electrodes are shown for demonstration purposes.

With the memristor arrays built on top of CMOS subsrates, a final photolithography step was carried out to open the I/O pads for electrical measurements. The Al I/O pads were exposed after RIE of the

TiOx/UV resist/TEOS stacking layer. The memristors were internally accessed through CMOS circuitry by applying voltages to the I/O pads surrounding each die on the CMOS chip. A custom built probe card which has 112 probes was used to apply voltage and to send measurement data to a PLT 1000 measurement system. The data acquisition was achieved by home made software that allows for individual control of each I/O pad. Using the memristor arrays as the data routing network, successful logic functions have been implemented in the hybrid circuits [10].

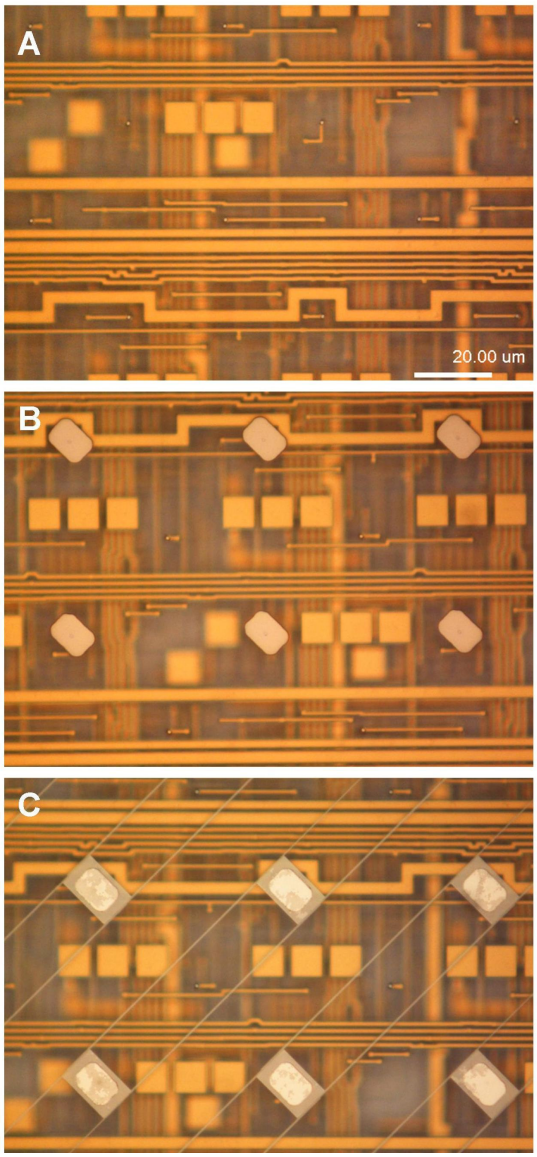

Figure 12: Optical images of the bare CMOS substrate (A) and the substrate with metal plugs (B). The metal plugs are connected with one set of W vias in CMOS after self-planarization and then the pads of the bottom electrodes (C) after the first NIL. All the three photos were taken with the same magnification.

4. SUMMARY

In this work, we have demonstrated the first hybrid memristor-transistor integrated. One big challenge was the large non-flatness (40-150 nm) of the CMOS substrate due to the 0.35 μm process. We developed and implemented three planarization techniques that reduced the non-flatness to <10 nm, and achieved successful nanoimprint lithography on top of the CMOS substrates, leading to the successful integration of memristors with transistors. The integration suggests that both memristors and their enabling technology NIL are compatible with traditional CMOS process. Moreover, the integration is a test vehicle for other potential applications of memristors such as non-volatile random access memory and neuromorphic network without changing the infrastructure in IC industry.

REFERENCES

[1]. Snider, G. S. and Williams, G.S., " Nano/CMOS architectures using a field-programmable nanowire interconnect", Nanotechnology 18, 035204 (2007).
[2]. Strukov, D.B. and Likharev, K. K., "CMOL FPGA: a reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices," Nanotechnology 16, 888-900(2005).
[3]. Strukov, D.B., Snider, G.S., Stewart, D. R. and Williams, R. S., "The missing memristor found," Nature 453, 80-83 (2008).
[4]. Chua, L.O., "Memristors-the missing circuit element," IEEE Trans. Circuit Theory CT-18, 507-519 (1971).
[5]. Yang, J.J., Pickett, M.D.,Li, X.M, et al., "Memristive switching mechanism for metal/oxide/metal nanodevices," Nature Nanotechnol. 3, 429-433(2008).
[6]. Wu, W., et al., "One-kilobit cross-bar molecular memory circuits at 30-nm half-pitch fabricated by nanoimprint lithography," Appl. Phys. A. 80, 1173-1178(2005).
[7]. Li, N.,"Application of nanoimprint lithography in nano-electronic devices," Ph. D. thesis. Princeton University, 2008.
[8]. Xia, Q., Yang, J. and Li, X., HP disclosure (2008).
[9]. Li, N., Wu, W. and Chou, S.Y., "Sub-20-nm alignment in nanoimprint lithography using Moire fringe," Nano Lett. 6, 2626-2629(2006).
[10]. Xia, Q., et al., submitted (2009).