Yield enhancement with DFM

Seung Weon Paek[a], Jae Hyun Kang[a], Naya Ha[a], Byung-Moo Kim[a], Dae Hyun Jang[a], Junsu Jeon[a]
DaeWook Kim[a], Kun Young Chung[a], Sung-eun Yu[a], Joo Hyun Park[a],
SangMin Bae[a], DongSup Song[a], WooYoung Noh[a], YoungDuck Kim[a], HyunSeok Song[a],
HungBok Choi[a], Kee Sup Kim[a], Kyu-Myung Choi[a]
Woonhyuk Choi[b], JoongWon Jeon[b], JinWoo Lee[b], Ki-Su Kim[b], SeongHo Park[b], No-Young Chung[b],
KangDuck Lee[b], YoungKi Hong[b], BongSeok Kim[b]

[a]Design Technology, [b]Technology Development
System LSI, Samsung Electronics Co., LTD., Yongin, Gyeonggi-do 446-711 South Korea

ABSTRACT

A set of design for manufacturing (DFM) techniques have been developed and applied to 45nm, 32nm and 28nm logic process technologies. A noble technology combined a number of potential confliction of DFM techniques into a comprehensive solution. These techniques work in three phases for design optimization and one phase for silicon diagnostics. In the DFM prevention phase, foundation IP such as standard cells, IO, and memory and P&R tech file are optimized. In the DFM solution phase, which happens during ECO step, auto fixing of process weak patterns and advanced RC extraction are performed. In the DFM polishing phase, post-layout tuning is done to improve manufacturability. DFM analysis enables prioritization of random and systematic failures. The DFM technique presented in this paper has been silicon-proven with three successful tape-outs in Samsung 32nm processes; about 5% improvement in yield was achieved without any notable side effects. Visual inspection of silicon also confirmed the positive effect of the DFM techniques.

Keywords: Design for Manufacturability, Yield Improvement

1. INTRODUCTION

Since 65nm Technology, the portion of yield loss due to systematic uncertainties has been increased rapidly and getting an acceptable yield on advanced technology nodes has become more difficult.

In order to overcome these difficulties Design for Manufacturing (DFM) technology has been developed. DFM, although convincing in theory, was considered difficult to implement to chip design since it tends to make the chip size increase and the benefits were difficult to quantify and measure. Most of EDA companies specializing in the DFM have gone out of business for this reason and the application of DFM techniques on real silicon has been limited in industry. At Samsung System LSI division, we combined a number of commercial available solutions and our internal developed capabilities into a comprehensive solution that can be applied to the design as library, IP and full chip in regular sequence and also as a way to correct designs afterwards. This breakthrough allowed for wide deployment of these DFM techniques on 45nm32nm and 28nm technologies nodes. The paper also discusses various quantitative analysis approaches performed with product level design and its silicon wafers to demonstrate benefits of DFM techniques and to determine the priority of given methodologies

In this paper, we introduce our DFM Prevention solutions, which include DFM kits, automated fixing, and DFM polishing in the part of post layout correction. Our DFM techniques has been applied to foundation IPs, analog and digital IPs and product level designs without noticeable overhead in area, silicon characteristics or design turnaround time. Also it is illustrated that additional application of our DFM techniques in physical, parametric failure analysis based on extracted test results from silicon.

Design for Manufacturability through Design-Process Integration VI, edited by Mark E. Mason, John L. Sturtevant,
Proc. of SPIE Vol. 8327, 832704 · © 2012 SPIE · CCC code: 0277-786X/12/$18 · doi: 10.1117/12.920029

1.1 The Trend of DFM development

As shown in Figure 1.1-1, roadmap of RET (Resolution Enhancement Technology) [1] [2] [3], one of important factor to address process difficulty show limitation of manufacturability around 45nm and beyond Technology [4]. At this situation, we can expect that process is hard to overcome less process margin with chip variation unless design helping. Thus, we began to consider DFM development from 65nm Technology. At initial stage for DFM development, only a few DFM kits are available for the layout optimization on standard cells in the Lib. Later on we have realized that DFM methodology is necessary as design flow to deploy process behavior well through DFM Prevention, Solution and Polishing into design.

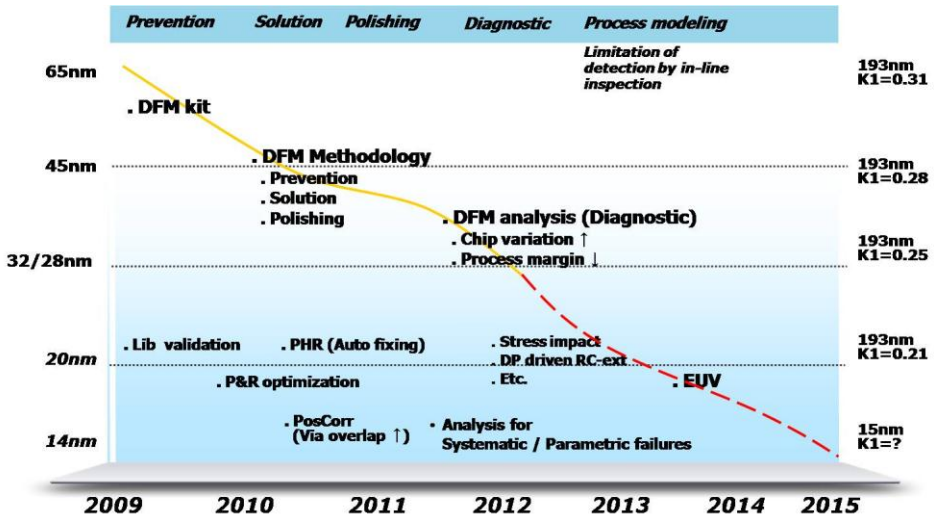


Figure 1.1-1. The trend of DFM Development.

In the DFM methodology, define a hotspot criteria and priority of correction with impact to yield among DFM applications is getting more importance for the efficient DFM adoption. Therefore, DFM analysis as diagnostic about results of silicon is required to feed back process behavior to design. Moreover, we anticipate this item as process modeling need to grow development for fine DFM analysis in extreme technology.

As of now, phase of DFM development are going to move from DFM methodology to DFM analysis. However, both approach must be coexist from design to silicon flow rather than separation.

1.2 DFM adoption in Process & Design timeframe

Most of a SoC (System on Chip) designs are composed with Lib. (Standard, Memory compiler & leaf cells etc.) and IPs, which have to be released earlier for the SoC design rather than matured process setup. So, defining a design or recommend rules [5] in period of rule base DFM are very important at the alpha process stage before DFM prevention (Lib. validation). DFM validations are proceeding with available DFM kits to make process-aware layout base on well-defined rules. For the IPs block design, optimization for P&R (Placed & Routing) tech file in the DFM prevention and DFM solution with silicon results are need a setup sequentially. If we lose this timeframe to integrate DFM application with design tools before release them to the designer for the IPs and Chip design, most of IPs are hard to refresh with DFM items later. It means that some of part such as Lib., IPs in the area of Chip design always doesn't adopted DFM items even if released to DFM methodology. Therefore, it is important that DFM prevention, solution on DFM methodology should be done completely within given timeframe in the design flow.

During process ramping-up stage with test chip design, which is already adopted by DFM application through DFM methodology, a lot of systematic, parametric failure analysis has been reported. At that time, carrying those results to design is one of significant flow for the complete design on DFM methodology. To do that, some of DFM application in the DFM methodology is required to prevent failures from silicon dynamically. Otherwise, there are a lot of known failures will be not care from design stage, although we know those failures can be increase load for process setup & less process margin.

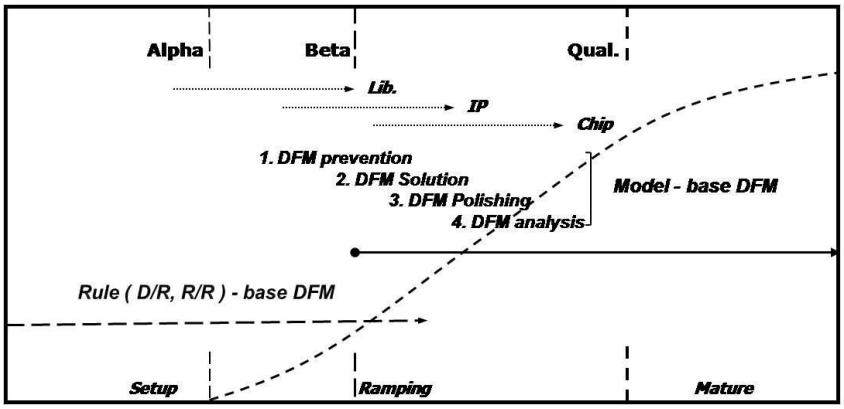
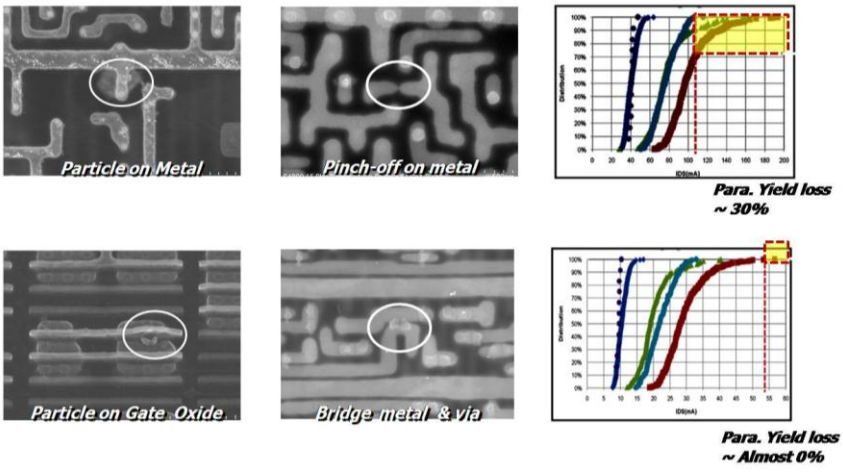


Figure 1.2-1. TimeLine for Technology development**.**

In case of rule base DFM, well-define a design rule include process behavior is very helpful and impact to designer rather than recommend rule in aspect of design view [5] [6]. Thus, defining a complete design rule with a lot of silicon results is important basis for better DFM realization. But because mismatch timeframe between define a rule and process development, model base DFM is require essentially to compensate weak points in rules. And model base DFM can carry efficiently with found failures on silicon to design stage. Most of 45nm, 32/28nm design in System LSI of Samsung have been optimized with addressed DFM methodology as shown Figure 1.2-1.

1.3 A type of failures

Generally causes of yield loss can be classified as random, systematic and parametric failures. Failures by particles during process as shown in Figure 1.3.-1 (a) were caused to connect problems directly. Those kinds of failures can be verified by pFA (Physical Failures Analysis) on silicon base on scan fail diagnostic results, but no available solution to prevent them from design stage even if found out root cause. However, we had accomplished less yield loss through reducing critical area by DFM prevention and will address at the section of 2.3 DFM prevention detailed.



(a) Random failures (b) Systematic failures (c) Parametric failures

Figure 1.3-1. Types of failures.

Most of systematic failures are relate with less process margin, which was layout or process scheme dependency generally. In past, most of systematic failure shows repeated hotspots on whole wafer due to fact that most of them were caused by explicit layout errors through OPC or MASK fabrication etc. While current systematic failures are detected on whole area of wafers randomly due to low process margin as shown in Figure 1.3-1 (b). Technical challenges must be

overcome to capture systematic failures on silicon with remarkable DFM analysis in the 45nm and beyond technology are require, which will address at the section of 3.1.1.

In order to get stable device characterization, operation should be within electrical target as leakage with given voltage etc. As shown at upper results in Figure 1.3-1 (c), only 70% of all measured results in the chip wafers are belong into leakage specification. While there are no measured data is out of specification at bottom results in Figure 1.3-1 (c).

Key problems in classifying 3 types failures [7] are analyzed a failure type with simulation by DFM kits and extract failure results from measured data. We propose to develop methodology for optimization of approaching as shown in Figure 1.4-1.

1.4 Approaching for Yield ramping up

In order to get target yield by process development, reducing period of ramping-up process with clean failures promptly are key issues. As main part of DLY (Defective Limit Yield), random, systematic failures are very populate at initial process setup stage. At that time, most of improvement for process focused to remove either random or systematic failures. According to the process improvement, drastically random failures are matured at certain timeframe in shown Figure 1.4-1, which can be controlled by process & restriction of equipment usage. Especially, finding root cause of systematic failures simultaneously are very important factor to reduce period of process ramping-up base on silicon results. If we know portion of systematic failure by various method, parametric failures easily can be estimate from measure yield results.

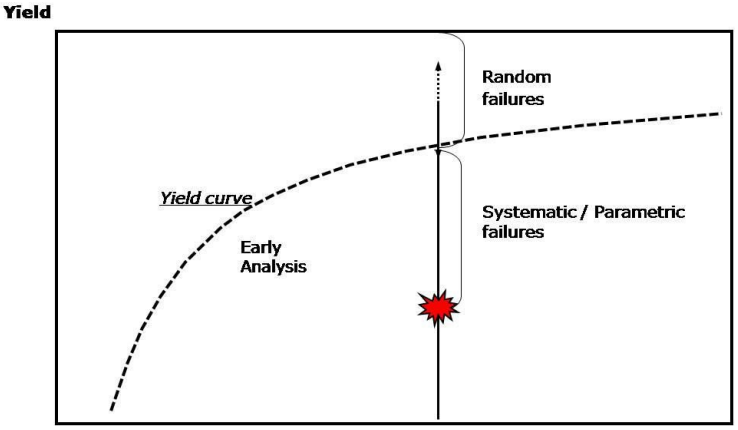


Figure 1.4-1. TimeLine for yield ramping-up.

In this situation, failures analysis faces challenge in developing capabilities to classify root cause of systematic and parametric failures and make a priority to correct among them by process or others. To analyze them efficiently, setup for automatic flow from silicon measurement (EDS; Electronic Die Store) to pFA is require. It also needs effort to define quantitative analysis to clarify systematic failures. These results will address with measured data on product level design at the section of 4.2.

2. DFM METHODOLOGY ON DESIGN STAGE

2.1 Silicon to design through DFM

Regarding conveys process information to design completely, it is not required only DFM kits but also DFM methodology should include prevention, solution and polishing to deploy well into design. At present most of process information for building DFM kits are deeply linked to physical design as layout due to fact layout can be modify by simulation before MTO (Mask Tape Out). Henceforth, we propose to develop electrical behavior-induced DFM kits (via implanting process and device simulation) for anticipated design targeting as one of new DFM kit.

All of transferable process information from process as weak patterns, variation of thickness and known hotspots etc. should be efficiently convey into Design Methodology through DFM kits [8], which are enable to design sequentially as shown in Figure 2.1-1.

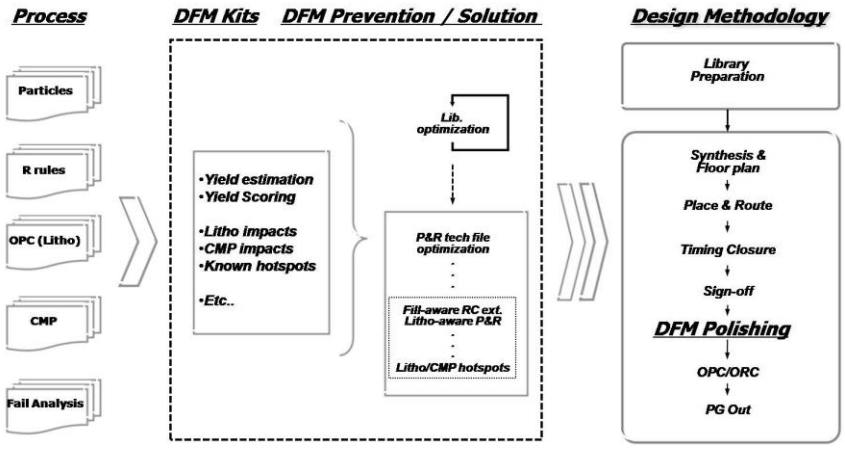


Figure 2.1-1. Flow from Silicon to design through DFM.

2.2 DFM kits

In Table 2.2-1, available DFM kits, which are commercial tool and internal built, are summarized in terms of Rule and Model base DFM kits.

Table 2.2-1. Kinds of DFM kits & those impacts.

Items	Model Base DFM kits			Rule Base DFM kits		
	Litho.	***CMP***	***CAA***	***Rule Scoring***	***PM***	***LUP***
Variables	OPC/RET	CMP / Dummy	Defect	Recommend Rules	Process (Litho ~ CMP)	Litho (General)
Hotspot type	Unknown (Modelized)		Statics	Known	Known (pFA / In-line inspection)	
Impact	Process margin ↑ Systematic failures ↓		Random failures ↓	Process margin ↑ Systematic failures ↓		
Feedback	Improving of Design or Process		Process	Improving of Design or Process		

1. Litho simulation → Validation for OPC recipe & Process behavior.
2. LUP (Litho Unfriendly Pattern) → Validation for litho-aware routing.
3. CAA (Critical Area Analysis) → Random Yield estimation.
   3-1. WCA (Weighted Critical Area) → Comparison of critical area by spreading / widening adoption in P&R
   3-2. Via counting → Checking about ratio of redundant via
4. PM (Pattern Matching) → Validation for process-aware routing
5. Rule Scoring → Validation for status of R-rule adoption
6. CMP (Chemical Mechanical Polishing) → Validation for thickness-aware routing with density status

During process setup & ramp up stage, some of random systematic manufacturing weak points can be identified. Generally, Model base DFM kits are useful to detect unknown hotspots and those results are needed for correlation between simulation and silicon to lead high confidentiality. Especially, CAA kit internally has a capability for calculation of double via counting and weighted critical area with distribution by particle size. While rule base DFM kits can be used in many ways as sign-off or verification on the design due to fact that those kits were built with confirmed or known hotspots, which were should be prevent from the silicon based design. And both of 2 types of DFM kits have an impact on the improve process margin and reduce random systematic failures through feedback to process or design stage in efficient way.

2.3 DFM Prevention

To draw layout restrictively for the process during design development, design rule, restriction by command or modify parameter in the design tools are very effective and efficient way in the current design flow. Except layout restriction by design rule, we realized that layout modification on custom design as standard, leaf cells etc directly with DFM kits and optimize design tool to build layout for process are powerful method. Additionally, those kind of work as DFM prevention set the stage for the DFM sign-off during designing so that layout should control the improved process. In our current approach, optimization of Lib. and P&R (Place & Routing) tech file are available and will be address at the section of 2.3.2 and 2.3.3.

2.3.1 Analysis for defect limited yield

As shown in Figure 2.3.1-1, both of 45nm and 32nm technologies are showed same trend of yield loss by particle. Analyzed results by CAA yield estimation, which was calculated by defect model base on measured data in the fab., showed that yield loss factor by particles are less yield loss on the BEOL (Back End of Line) than FEOL (Front End of Line).

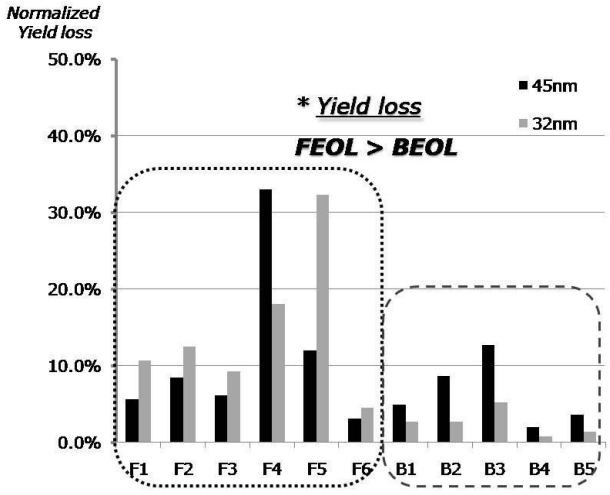


Figure 2.3.1-1. Status of yield loss by area with Technology

In these convinced results, Lib. (Standard, Leaf cells and I/O etc.) validation turn out to be meaningful step in the design flow. However, we should not overlook the main factor about yield loss on the bit cells of memory. Thus, optimization in given process status of design rules for bit cell drawing at the earlier design stage is emphasizing again.

In case of 32nm in Table 2.3.1-1, yield loss on the BEOL is relatively less than FEOL. We assumed that less yield loss at the BEOL of design was caused by application of DFM prevention. Hence, optimization of P&R tech file for the process-aware layout is becoming a main method to improve random or systematic failures, which will address respectively at the section of 2.3.3.1 and 2.3.3.2. Approximately both of 45nm and 32nm technologies are showed same trend of yield loss by particle with slimier reason on the FEOL and BEOL

2.3.1-1. Ratio of Normalized Defective Yield loss

	45nm		32nm	
	SRAM	**Logic**	**SRAM**	**Logic**
FEOL	4.9	2.1	6.1	2.6
BEOL	3.0		1.3	

2.3.2 Validation for Custom design (Standard, Leaf cells & I/O etc.)

One of the difficulties associated with application of DFM techniques is conflicting rules. It is difficult to determine which application is enough without incurring unacceptable overhead. Another big obstacle is the application timeframe adds to the overall design phase.

Generation of double contacts in the standard cells is allowing area within rule constraint. It is beneficial way to minimize damage of particles in terms of characterization or yield. When layout modifying to insert double contact, it should be considered overlap margin significantly with other layers. If not, characterization of standard cells can be take turn for worst after integrated all of cells on the chip.

We were able to generate one Figure of merit based on a proprietary technique of combining the benefit of various recommended rules. The recommended rules have been placed into five different categories based on their benefit to yield. This calculation has been integrated into the scoring kit is available commercial solution. Based on customized guideline we were able to provide automatic application of DFM guideline for standard cells and other custom design as leaf cells, I/O and peripheral of the Memory blocks etc.

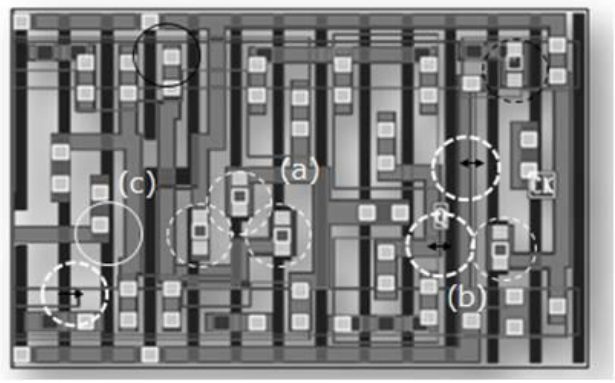


Figure 2.3.2-1. Standard cell in 45nm. (a) Double contact. (b) Recommend rule (c) Litho

Finally, litho simulations require modifying layout by litho behavior [9] [10]. Without no weak patterns occurred include process variation.

After optimization, scoring used to validate optimization indeed result in improvements from view of scoring [11] [12]. For the verification, hundreds of cells in 45nm library have optimized using validation flow and the results of score improvements are shown in Figure 2.3.2-1.

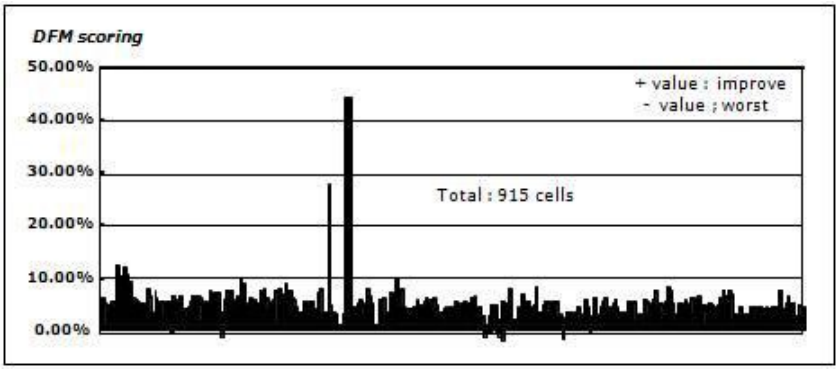


Figure 2.3.2-2. Verified results by Rule scoring after validation on 45nm standard cells

Improving scoring, maximum 43.89% with the average of 4.31%, among cells were confirmed [13]. The benefits of DFM have been validated on Silicon, which will address at the section of 5.2.in conclusion. More significantly, the prediction of yield improvement by the Scoring was observed similar results on silicon. This reflect quite remarkable index given that industry in general really has no way of quantifying benefit of DFM techniques.

2.3.3 Optimization of P&R tech file

Full chip level optimization involves BEOL as opposed to FEOL optimization done by library optimization. One important consideration for full chip level optimization doesn't result in full chip timing changes as this could result in going through design iterations to achieve manufacturability while meeting the specification of timing. The approach we took involves achieving the DFM optimization without timing distortion. This was achieved by integrating DFM changes into P&R tools as "tech files". This allowed for us to optimize metal layers of designs without adding the design iterations. Any DFM requirements that couldn't be achieved this way are later corrected with what we call, DFM polishing at the section of 2.5.

2.3.4 LUP (Litho Unfriendly Pattern)

Due to RET limitations in 45nm and 32/28nm technologies nodes, there are more significant patterning issues in this node. These issues can happen even if there are no DRC (Design Rule Check) violations. LUP prevention technique in the P&R tech file looks for specific patterns that are known to make difficulty for RET and avoids generation of these types of patterns during P&R phase. LUP should be defines carefully to minimize affection of P&R runtime due to there are a lot of LUP detected & correction during design by P&R. Most of defined LUP, which are general litho unfriendly pattern to prevent from design fundamentally, it can be candidate as weak pattern with wide range of process variation. Figure 2.3.3.1-2 is one of example results on metal2 of 32nm product level design before routing with optimized tech file.

Base on expertise accumulated in process development including OPC (Optical Proximity Correction) step, there are few types of LUP that we avoid using "tech files" of P&R. When P&R tech file was setup at initial design stage, NBH-END, H, U-shape are not considerable items for the improved timing closure unless getting feedback from process. In the Figure 2.3.3-1, show what type of shape on routing is caused to weak pattern as bridge, pinch etc with less process margin and status of correction for U-shape after optimization of P&R tech file. We confirmed on silicon that there are no doubts about helpful for the improving process margin by DFM prevention. However, current DFM prevention is still insufficient data gathering to drive designer. Therefore DFM analysis as section of 3.1.1 is require developing in a short time.

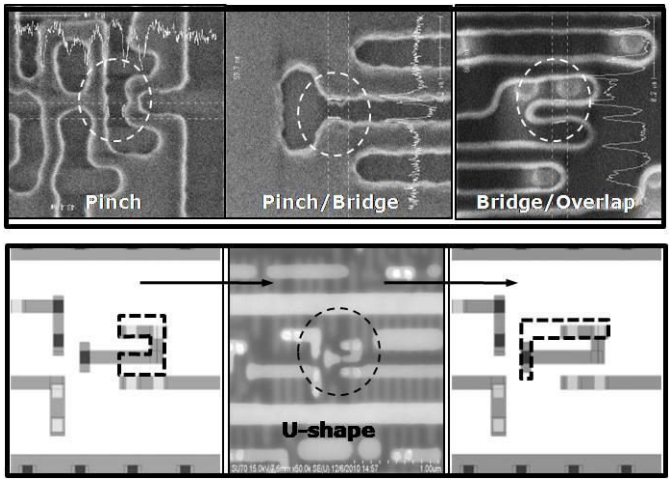
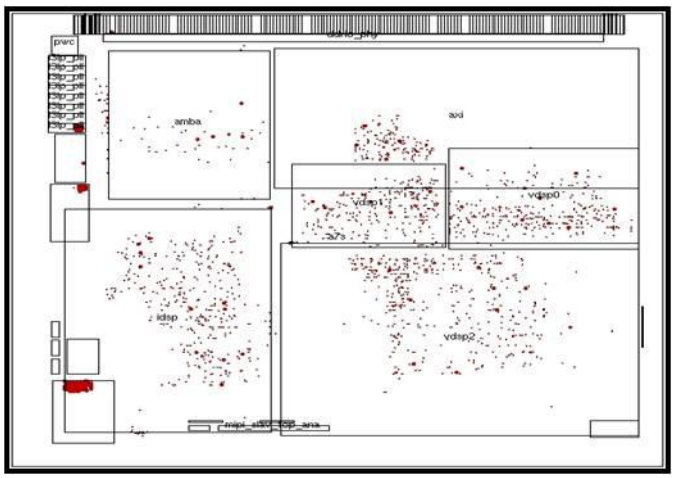


Figure 2.3.4-1. LUP (Litho Unfriendly Pattern) & status of correction for U-shape.

Generally P&R tool has been used for field of digital design extensively from various IPs include mixed block with analog and top block of Chip. Hence, optimized tech file should be applied from IP level to prevent all kind of LUP to make complete chip with cleaned LUP as shown in Figure 2.3.3.1-2.

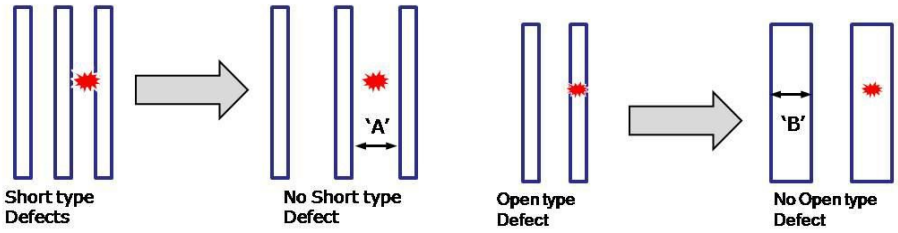


(a) NBH_END (544 ea), (b) H-Shape (63,549 ea), (c) U-Shape 15,649 ea
Figure 2.3.4-2 Status on M2 without LUP adoption in 32nm design

Hence, Technical challenge that must be overcome to reduce gap of timeframe to predetermine LUP with forecasting process behavior in advance IPs design on the earlier process status before gathering silicon results during new technology development.

2.3.5 Metal widening & spreading

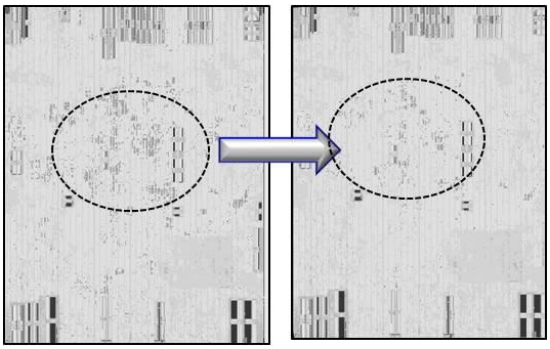
As mentioned above at the section of 2.3.1, it is important to prevent less yield loss by particles through reduce critical area on design. However, degradation of litho process margin on generated jog pattern by method of widening and spreading as shown in Figure 2.3.3.2-1. This step should be considered when optimize parameters are widening and spreading in tech file from P&R tools.



(a) Wire spreading (b) Wire widening

Figure 2.3.5-1 Optimize Wire spreading & widening

Analysis BEOL routing layout shows most of yield loss factor by particles are caused to metal short/open failures in the Table of 2.3.1-1 (Normalized yield loss on 32nm design: 1.3). To improve these empirical results, metal widening with spreading has been applied to routing layout, which is able to reduce critical areas as reported by the CAA kit.



(a) Beforehand (b) Afterward

Figure 2.3.5-2 Status of before & after application

Creating advanced wire spreading and widening as shown Figure 2.3.3.2-1 In order to prevent litho hotspot required optimization for minimum jog length, space and jog widening. We selected around 1.5x spreading / widening whenever possible. We can check how much critical area changed on simulation map between beforehand and afterward as shown in the Figure 2.3.3.2-2 approximately.

2.3.5-1. Yield estimation (Simulation) depends on weighted critical area on design.

	Weighted Critical Area (Design)	Yield (Simulation)
Metal SHORT ('A')	1.5%↑	0.1%↓
Mental OPEN ('B')	7.7%↓	0.7% ↑

As shown in Table 2.3.3.2-1, we observed the increase in yield estimation is 0.7% by decrease 7.7% in critical areas for Metal open and also decrease 0.7% yield estimation by decrease 1.5% in critical area without any side effects that would require design iterations on ECO (Engineering Change Order) stage in the design flow. This solution applied on a 45nm test design (Over 10,000um x 10,000um) and confirmed 0.7% yield.

2.4 DFM Solution

Conceptually, DFM validation and Prevention are very effective approaching to make robust physical design exclude design rule generation, which is highest priority to restrict layout drawing among known method in my knowledge.

However, some solution during designing step become necessary to represent process behavior dynamically as found any failures on silicon or changing of process specification during process ramping-up. Product level design requires revision in many times due to process condition or design update etc until meet target characterization with process margin or yield. In that time, optimizing BEOL on the design is best way to convey process situation of those day to design naturally from DFM methodology. Of course, those results by DFM solution must be no affects from any physical information as size of chip.

2.4.1 Process Hotspot Repair

Although we were able to generate optimized tech files from P&R tools in the DFM prevention as mentioned above, it is difficult to prevent all litho hotspots completely. It is possible to do additional PHR (Process Hotspot Repair) as well as Litho-aware P&R just for the purpose of removing litho hotspots. In 45nm design and below chip design, PHR application in the DFM solution has been adopted during ECO phase as a way to remove difficult to correct litho hot spots. Figure 2.4.1-1 shows how this approach fixes one of the litho hot spots with PM library [14] [15] [16] [17].
As the result of applying a new method to 32nm chip design, the average rate of fixing hotspots of 1x metal layers on chip design is over 95%, if PHR was applied 2 times at least at almost last ECO stage. Although process hotspot is fixed, we had confirmed that there are no notable timing violations, when result of timing closure was compared [18].

As a result, we realized this solution also reduces burden from OPC step as it removes OPC hotspots from the design itself before the OPC step.

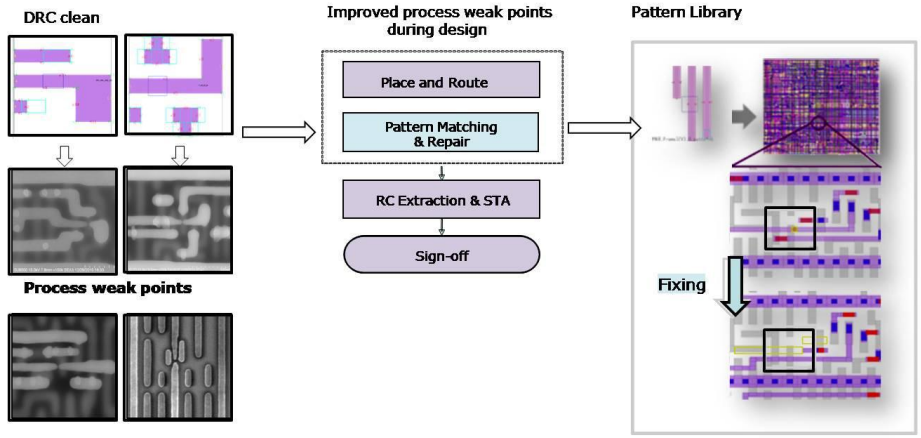
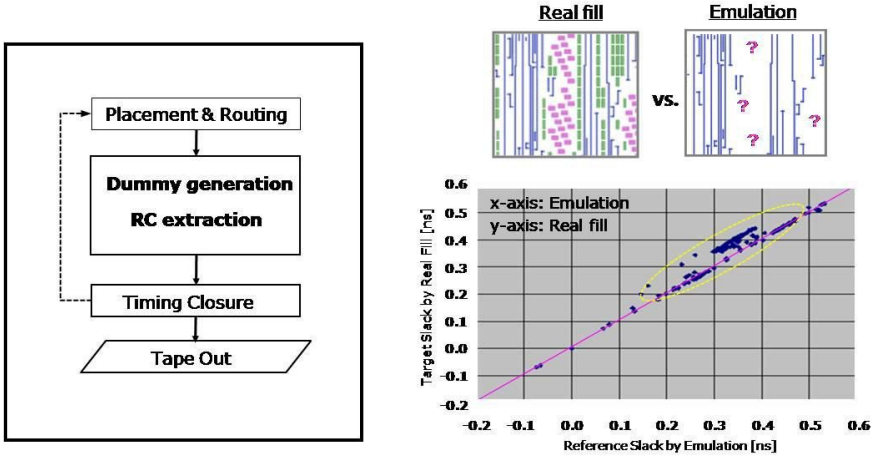


Figure 2.4.1-1. PHR (Process Hotspot Repair) flow on ECO

2.4.2 Fill-aware RC extraction

Another application of DFM solution is in the area of timing analysis. Advanced extraction of RC parameters using metal fill (or dummy) can provide much more accurate, needed and timing model using this methodology.



(a) Fill-aware RC extraction flow (b) Slack difference between Real fill & Emulation

Figure 2.4.2-1. Fill impact on timing closure

Previously RC extraction flow used to emulate information. Actually emulated base RC extraction was well known method to calculate resistance and capacitance from previous technology. Adding conservative guard-band to compensate for this inaccuracy would weakens competitiveness of design in smaller node technology the flow shown in Figure 2.4.2-1 (a) allows accurate RC parameter extraction considering actual metal fill effects [19]. However, emulation base extraction faces challenge with the scaling of technology since 45nm node. Through timing simulation, it was proven the inaccuracy of emulated fill over 5.0% at 45nm and over 6.0% at 32nm in terms of capacitance with test design.

Under tight specification for timing closure, we had verified timing difference results between real fill and emulation base extraction as shown in Figure 2.4.2-1(b). As we expect, meaningful difference has been confirmed on simulation precisely, which turn out fill-aware RC extraction can carry realistic process behavior to design.

2.4.3 Chip validation

Our DFM technology found applications outside of intended DFM methodology. The flow used in the area of process monitoring point identification, physical Failure analysis, timing analysis and test quality improvements.

In logic process, it is difficult to predict manufacturing weak spots that would give a good indication of process development. Our flow for DFM validation can use combination of DFM kits to identify known and unknown hotspots for a given design. These hotspots are used by FAB to monitor potential weak points during manufacturing so any process shift results in yield excursion can be caught early and corrected in early stage. As mentioned, many built DFM kits are used for this purpose as shown in Figure 2.4.3-1.

To detect various encounter hotspots during process on layout, there are many type of DFM kits are available. Typical model base DFM kits as Litho, CMP and CAA kit has used for unknown hotspot detection [20] [21] [22] [23] on design as mentioned in Table 2.2.-1. And rule base DFM kits as Rule scoring, Pattern Matching and LUP kits used for known hotspots with pattern library base on silicon results.

As process feature sizes decreases, DFM validations process largely require before for process monitoring and development. These results will give benefit to reduce MASK revision & spending time for inspection.

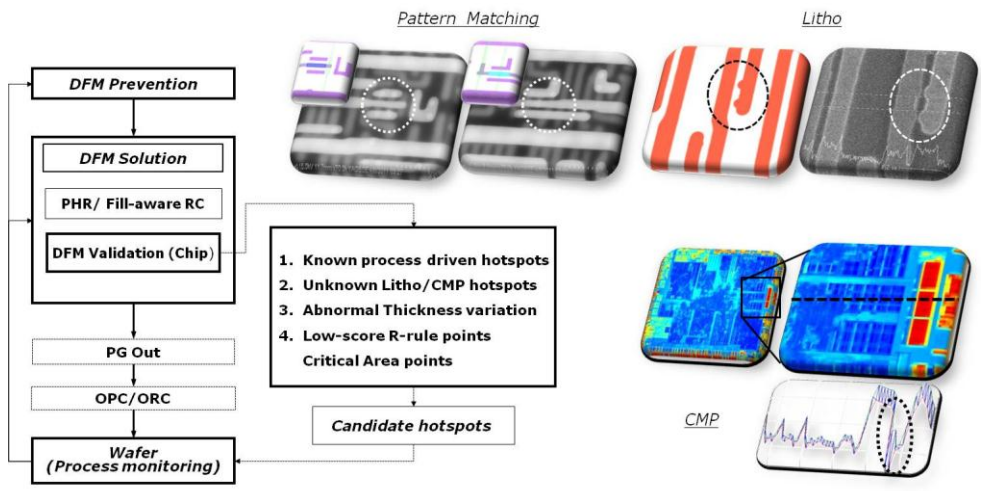


Figure 2.4.3-1. Chip validation with various DFM kits.

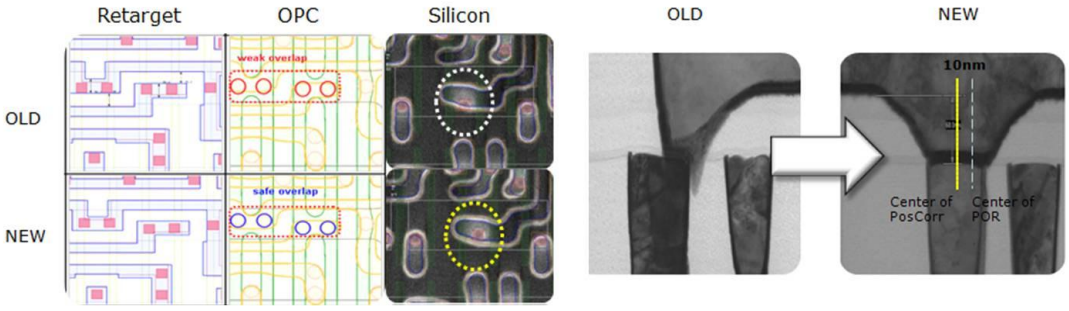
2.5 DFM Polishing

Even after all design for manufacturing features in place as part of regular sign-off design flow, there are residual weak spots at the end of the design. These are addressed with layout optimization, which design to have no material effect on timing within designer intent.

2.5.1 Via Position Correction

In-line CD images in OLD section of Figure 2.5.1-1 (a) shows the effect of OPC shifting placement of metal lines. The metal lines have shifted as resulted of asymmetric bias during OPC and corner rounding by limitation of optics during patterning. This resulted in misalignment of vias as shown in OLD section of Figure 2.5.1-1 (b) generating manufacturing weak spots.

In cases where there are no room to apply symmetric bias, OPC (optical proximity correction)-aware design polishing can nudge the placement of vias to better align intended features as displayed in NEW section of Figure 2.5.1-1 (a), (b). This is done without any design rule violations and no material impact on timing. This made possible by the intelligent tool that is aware of OPC characteristics.



(a) Status of via overlap by Old & New method (b) Side view of overlap status after adoption

Figure 2.5.1-1 Via position Correction

The enhancement of overlap margin by Position Correction method has been validated by SEM image in section of Figure 2.5.1-1 (a). Even if limitation of controlling on silicon is difficulty, this technique has been applied to 1x all via layers on 32nm product level design and derived to actual yield improvement, which will address at the section of 5.1. This result actually signifies over 85% reductions of defects in that layer. Hence, we expect that this method is to significant yield improvements.

3. DFM DIAGONOSTIC ON SILICONS

3.1 DFM Analysis

DFM in semiconductor industry faces tremendous challenge with yield results in each DFM application on design flow. Although spending many efforts to deploy DFM methodology, all of DFM items could not exist anymore in the design flow unless shows quantitative results by applied items.
Thus, we have trying to find out any impacts analytically with various considerable methodologies for the systematic and parametric failures. Regarding approaching and its results are introduces well in section of 3.1.1 and 3.1.2.

3.1.1 Analysis of Systematic failures

It is very difficult to get causes of systematic failures in logic area. Most of the logic process yield ramp is done with SRAM. There have been suggesting of using DFM guidelines for systematic yield loss analysis [24] but we have applied DFM in yield learning in a fundamentally new way.
The flow for analysis of systematic failures on logic area contains overlay analysis among candidate nets from scan fail diagnosis, candidate hotspots from DFM validation and defect coordinates from in-line inspection, which is a CD SEM image taken during manufacturing that can indicate suspected defect locations. Hypothesis for yield drop or historic knowledge of potential yield loss mechanisms can be translated to DFM hotspots using our DFM methodology. This approach tries to reach much further than commercially available capabilities what we tried to find the repeated commonality among failures. The resulting overlay analysis is presented statistically. This kind of overlay analysis is also very useful in prioritizing hypothesis of yield drop and in predicting yield increase by process improvement.

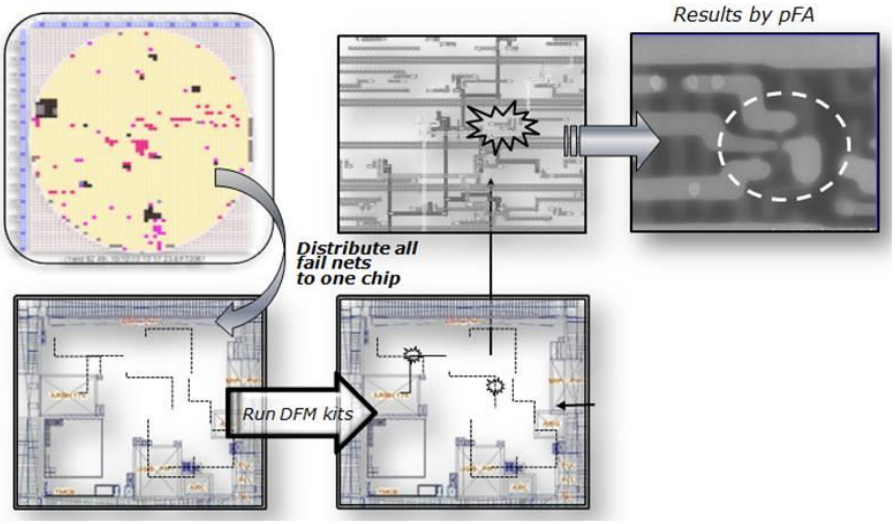
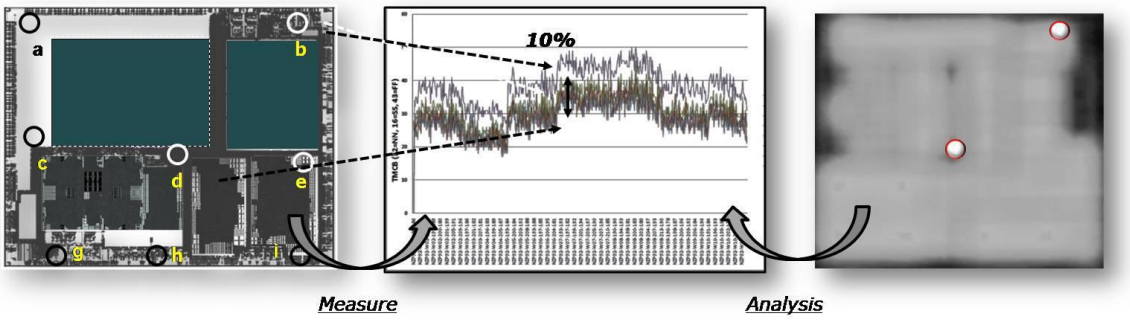


Figure 3.1.1-1. Wafer level inspection with fail nets to enable efficient pFA

In 32nm technology device flow was used and validated as shown in Figure 3.1.1.-1. In the near future, the flow is expected to identify root causes of yield loss based only hotspot information from results of our DFM validation or accumulated expert database with known systematic failures. This flow will also be use identifying impact or assuming priorities of yield loss by kind of hotspot.

3.1.2 Analysis of Parametric failures

It is important to monitoring parametric results as Vth, frequency etc. to find out root causes of parametric failures in each location of chip. Ideally, all of these results must be identify every location on chip. However, we already knew this results are different depend on location of chip due to OCV (On chip variation) by process. Hence, unique circuits for monitoring to accurate and fast measurement about parametric behavior on the chip come into request.



(a) Location IP for monitoring on Chip (b) Difference of center / edge Vth (c) Density map of dummy on chip
Figure 3.1.2-1. Volume monitoring for electrical behavior variation.

This monitoring IP include special circuit inside chip to able to monitor easily the parameter change as device again, AC performance (die to die, wafer to wafer & lot to lot variation / excursion) and processed output as loading variation, transistor Vth variation and process excursion warning. For this purpose, RO (Ring-oscillators) has been adopting widely in semiconductor industry. 13% on chip delay variation discovered on 32nm product level design at the center / edge of chip as shown in Figure 3.1.2-1. Based on these results, finding root causes of phenomena and effort to remove them by process controlling and design changing respectively. Currently this monitoring IP is being applied to all products on in entire technology for the higher yield.

4. DFM ASSESSEMENT

4.1 Status of adoption about DFM items

To verify DFM impact with yield on silicon, we applied to establish DFM methodology and analysis to both of blocks in the chip level test design as shown in Figure 4.1-1.

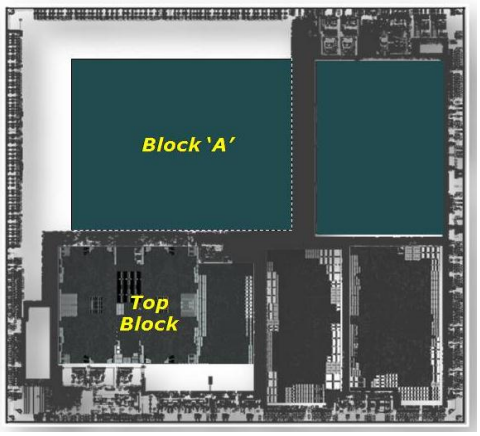


Figure 4.1-1. Test design for DFM adoption

3 of 8 items have been applied 2 types of design identically due to those DFM application is common methodology in that time. Except Lib. validation in the DFM prevention stage, most of DFM application is related with BEOL for optimization. Especially, LUP, PHR and Position correction has been developed with pFA results, which was already turn out one of yield detractor.

Table 4.1-1Difference of DFM adoption

	Items	No adoption	Adoption
DFM Prevention	Lib. Validation	○	○
	LUP	**X**	○
	BARVIAs	**X**	○
	Metal spreading	**X**	○
DFM solution	Process Hotspot Repair	**X**	○
	Real fill aware RC extraction	○	○
	DFM validation	○	○
DFM polish	Position Correction	**X**	○

4.2 Comparison of result by DFM adoption

As shown in Table 4.2-1. All of DFM applications improved result between before and after adoption. LUP application is superior results than others due to not allowing any generate LUP during routing process. Therefore, LUP can be removes efficiently. In these results, we recognize optimization of P&R tech file is one of best way to restrict BEOL for process-aware design. Position correction method was applied to both of design on data preparation stage. This application shows correction of detected miss-aligned via with metal to compensate OPC behavior.

Table 4.2-1. Analysis result by DFM kits

`	No adoption	Adoption	Remark
LUP	1,280,589	8,624	99.3% remove
Redundant via ratio	47,916,834	37,496,321	~ 21.7% reduction
Wire spreading	4,860,376	4,827,034	~ 0.7% reduction
Pattern Matching	312,005	27,907	~ 91.1% removal
Litho simulation	0	0	No Critical hotspots
Position Correction	73,743,421 → 16,648,666		~77.4% correction

The 2nd design with improved design by DFM adoption has been obtained 30.3% gain (ratio) of DLY compared to 1st design with no DFM adoption. And also Top block show more yield improvement in proportional to area of block. According to these results, we assumed that yield improvement is relates with amount of applied DFM application in given area of design. However, we did not assure yield result in table 4.2-2 is come from DFM adoption. But, just we believe that part of yield improvement

Table 4.2-2. Gain (Ratio: 1st vs 2nd) of Defective Limit Yield by DFM adoption

Category	Block	Item	Gain (Ratio : 1st vs 2nd)
Defective Yield loss			30.3%↑
SCAN (Logic)	Top Block	Shift	3.2%↑
		Capture	68.3%↑
	Block 'A'	Shift	46.5%↓
		Capture	99.0%↑

Practically, we needed DFM analysis whether how much systematic and parametric failure was remove by DFM application. Then, we can assure DFM benefit and push to deploy DFM methodology to design, even if TAT is increasing.

5. CONCLUSION

5.1 Adopted DFM results on silicon

Since 45nm technology, Samsung has been developing DFM kits, Prevention, Solutions and Polishing methods fit with each technology using overall DFM methodology. Unlikely our competitors, Samsung enable automatic fixing of library cells without increasing the area of the cell. Full chip levels DFM solutions are also unique to Samsung and allow extensive use of DFM techniques at 45nm, 32nm, and 28nm technology node.

Table 5.1-1. Result of yield enhancement by DFM items.

	Items		Yield Enhancement (Silicon base)
DFM Prevention	Lib. validation		**Alpha** ↑ * Verified yield enhancement on 45nm test design
	BEOL optimization (P&R)	LUP	
		BARVIAs	
		Spreading	
DFM solution	Process Hotspot Repair		**Beta**↑ * Prevent yield loss directly * Timing accuracy ↑ * For process monitoring
	Real fill aware RC extraction		
	DFM validation		
DFM polishing	Position Correction		**Gamma** ↑ * Potential yield enhancement
DFM Analysis	Systematic failures		**Delta** ↑ * Assessment about yield impact
	Parametric failures		

As shown in Table 5.1-1, DFM prevention show proven yield about alpha through compare 2 type (DFM vs No DFM) 45nm design and possibility to prevent detractor of yield loss absolutely. It is very important way to prompt process ramping-up with removing systematic failures, if we can prepare known hotspot from silicon as many as possible. As we mentioned, DFM solution is one of dynamic solution to represent process behavior during design. By DFM analysis, fixed hotspots by PHR are causing to yield loss during process setup at that time. It means that PHR enable to yield-up about 8.0% to the contrary. We believe real fill-aware RC extraction is assured to represent realistic process variation for

the accurate timing closure. Since process improves very rapidly, removing systematic failure is one of urgent priority. We realized results of DFM validation before MTO is very helpful for efficient process development. Finally, DFM polishing is very helpful to compensate OPC behavior and verify an accomplishment on the silicon. In our knowledge, this application in the DFM polishing is getting more required in beyond technology.
We propose to DFM methodology (prevention and solution via DFM simulation and silicon results) and analysis (root cause of systematic, parametric failure via DFT, DFM results) approaches to implement process-aware design, and design optimization to minimize process-induced weak pattern and to maximize process gain, for yield improvement in the sub-45nm, 32/28nm technology. The impact of DFM on device performance will be increasing gradually. This work will directly address the grand challenge of Logic Device Scaling to help pave a pathway for future sub-micron technology development essentially.

5.2 Future work

So far, DFM techniques have focused on layout optimization in aspect of reduce systematic and random defects. Most of designers are asking questions about design impact and yield data before they adopt DFM methods. They still have a doubt about any improvement by DFM application. For better clarification, we have to consider new DFM kits to check electrical behavior, improved DFM kits for wafer level simulation and quantitative analysis in each DFM application are required by various DFM analyses through diagnostic with DFM kits.
Finally, all of DFM methodology must be provided in right timeframe with sufficient technical evidence to be essential solution.

REFERENCES

[1] C. Mack, Fundamental Principles of Optical Lithography. New York: Wiley, 2007.
[2] Schellenberg, F.M." Design for Manufacturing in the Semiconductor Industry : The Litho / Design Workshops, VLSI Design, 1999. Proceedings. Twelfth International Conference On 7-10 Jan. 1999 Page(s):111 – 119.
[3] L.W. Liebmann, "Layout Impact of Resolution Enhancement Techniques: Impediment or Opportunity", Proc. ACM/IEEE Intl. Symp. on Physical Design, 2003, pp. 110-117.
[4] Mark E. Mason " DfM EDA Technology : A Lithographic Perspective " Symposium on VLSI Technology Digest of Technical Papers, June(2005), page : 90-91.
[5] Maynard, D.N.; Runyon, S.L.; Reuter, B.B. "Yield Enhancement Using Recommended Ground Rules " Advanced Semiconductor Manufacturing, 2004. ASMC '04. IEEE Conference and Workshop, 4-6 May 2004 Page(s):98 – 104
[6] W. Hoppe, T. Roessler, J. A. Torres, "Beyond rule-based physical verification," Proc. SPIE (2006), vol. 6349, no. 190.
[7] Chiang, C.; Kawa, J. "Three DfM Challenges: Random Defects, Thickness Variation, and Printability Variation " Circuits and Systems, 2006. APCCAS 2006. IEEE Asia Pacific Conference on, 4-7 Dec. 2006 Page(s):1099 –
[8] J.A. Torres, "Litho-friendly design: a necessary complement to RET", Microlithography World, vol. 15, no. 2, pp. 10, 12-13A, May 2006.
[9] K. Peter, R. März, and S. Gröndahl, "Litho-Friendly Design (LFD) methodologies applied to library cells," Proc SPIE (2006), vol. 6349, no. 14.
[10] L. Capodieci, "From optical proximity correction to lithography-driven physical design (1996-2006): 10 years of resolution enhancement technology and the roadmap enablers for the next decade," Proc. SPIE (2006), vol. 6154, no. 1.
[11] Daehyun Jang et al, "DFM optimization of standard cells considering random and systematic defect," ISOCC Int. Conf., vol. 01, pp.I-70–I-73, 2008
[12] Robert Aitken, " DfM Metrics for Standard Cells " proceedings of the 7th International Symposium on quality Electronics Design (ISQED'2006).
[13] Seung Weon Paek; Dae Hyun Jang; Joo Hyun Park, Naya Ha, Byung-Moo Kim et al., "Enhanced layout optimization of sub-45nm standard: memory cells" , SPIE (2009), Vol. 7725,72751M
[14] V. Dai, J. Yang, L. Capodieci, N. Rodriguez. DRC Plus: Augmenting standard DRC with pattern matching on 2D geometries. Proc. SPIE (2007), vol. 65220A.
[15] Jae-Hyun Kang et al, "Combination of rule and pattern based lithography unfriendly pattern detection in OPC flow", Proc. of SPIE Vol. 7122,(2008)

[16] Vito Dai, L. Capodieci, Jie Yang, N. Rodriguez, "Developing DRC Plus Rules through 2D Pattern Extraction and Clustering Techniques" Proc. SPIE (2009), vol. 7275, no. 727517.
[17] Justin Ghan, Ning Ma, Sandipan Mishra, Costas Spanos, Kameshwar Poolla, Norma Rodriguez, Luigi Capodieci, "Clustering and pattern matching for an automatic hotspot classification and detection system", SPIE (2009) Vol. 7275, 727516.
[18] J. H. Park, S. W. Paek, Naya Ha, D. H. Jang, B. M. Kim, H. S. Won, and K. M. Choi, "Fixing lithography hotspots on routing without timing discrepancy", International SoC Design Conference , 2009, p33-36
[19] Andrew, B. Kahng, and K. Samadi, "CMP fill synthesis: A survey of recent studies," IEEE Trans. Computer-Aided Design, vol. 27, no. 1, 2008.
[20] Convergent automated chip-level lithography checking and fixing at 45 nm, Valerio Perez, et al. , Proc. SPIE 7275, (2009)
[21] Mark C. Simmons, Jae-Hyun Kang, Youngkeun Kim, et al., "A state-of-the-art hotspot recognition system for full chip verification with lithographic simulation", SPIE (2011), Vol. 7974, 79740M
[22] Mark C. Simmons, Jean-Marie Brunet, Seung-Weon Paek, et al., "System to improve RET-OPC production by dynamic design coverage using sign-off litho simulator", SPIE (2008), Vol. 6925, 69250X.
[23] Naya Ha, Jinwoo Lee, S. W. Paek, et al., "In-design DFM CMP flow for block level simulation using 32nm CMP model", SPIE(2011), Vol. 7974, 79740W.
[24] M. Keim, N. Tamarapalli, H. Tang, M. Sharma, J. Rajski, C. Schuermyer, and B. Benware, " A Rapid Yield Learning Flow Based on Production Integrated Layout-Aware Diagno-sis", International Test Conference, 2006, p1-10–