Device-correlated metrology for overlay measurements

Charlie Chen
George K. C. Huang
Yuan Chi Pai
Jimmy C. H. Wu
Yu Wei Cheng
Simon C. C. Hsu
Chun Chi Yu
Nuriel Amir
Dongsub Choi
Tal Itzkovich
Inna Tarshish-Shapir
David C. Tien
Eros Huang
Kelly T. L. Kuo
Takeshi Kato
Osamu Inoue
Hiroki Kawada
Yutaka Okagawa
Luis Huang
Matthew Hsu
Amei Su

Device-correlated metrology for overlay measurements

Charlie Chen,[a] George K. C. Huang,[a] Yuan Chi Pai,[a] Jimmy C. H. Wu,[a] Yu Wei Cheng,[a] Simon C. C. Hsu,[a] Chun Chi Yu,[a] Nuriel Amir,[b] Dongsub Choi,[c] Tal Itzkovich,[b,*] Inna Tarshish-Shapir,[b] David C. Tien,[d] Eros Huang,[e] Kelly T. L. Kuo,[e] Takeshi Kato,[f] Osamu Inoue,[f] Hiroki Kawada,[f] Yutaka Okagawa,[f] Luis Huang,[g] Matthew Hsu,[g] and Amei Su[g]

[a]United Microelectronics Corporation, Fab12 Engineering, No. 18, Nan-Ke 2nd Road, Science-based Industrial Park, Hsin-Shi, Tainan 744, Taiwan
[b]KLA-Tencor Israel, Optical Metrology Division Application, 1 Halavyan Street, Migdal Ha'emek, 23100, Israel
[c]KLA-Tencor Korea, Optical Metrology Division Application, 7th Floor Star Plaza Building 92-7, Bansong-dong, Hwasung, Gyeonggi-do 445-160, Republic of Korea
[d]KLA-Tencor Corporation United States, Optical Metrology Division Application, One Technology Drive, Milpitas, California 95035, United States
[e]KLA-Tencor Taiwan, Optical Metrology Division Application, Tai Yuen Hi-Tech Industrial Park, No. 22 Taiyuan Street, Zhubei, ChuPei, HsinChu, Hsien, Hsinchu 302, Taiwan
[f]Hitachi High-Technologies Corporation Japan, Metrology and Inspection Division, 24-14, Nishi-Shimbashi 1-chome, Minato-ku, Tokyo 105-8717, Japan
[g]Hitachi High-Technologies Taiwan Corporation Taiwan, 1F, No. 12, Lane 31, Section 1, Huandong Road, Xinshi, Shiang, Tainan 744, Taiwan

Abstract. One of the main issues with accuracy is the bias between the overlay (OVL) target and actual device OVL. In this study, we introduce the concept of device-correlated metrology (DCM), which is a systematic approach to quantify and overcome the bias between target-based OVL results and device OVL values. In order to systematically quantify the bias components between target and device, we introduce a new hybrid target integrating an optical OVL target with a device mimicking critical dimension scanning electron microscope (CD-SEM) target. The hybrid OVL target is designed to accurately represent the process influence on the actual device. In the general case, the CD-SEM can measure the bias between the target and device on the same layer after etch inspection (AEI) for all layers, the OVL between layers at AEI for most cases and after develop inspection for limited cases such as double-patterning layers. The results have shown that for the innovative process compatible hybrid targets the bias between the target and device is small, within the order of CD-SEM noise. Direct OVL measurements by CD-SEM show excellent correlation between CD-SEM and optical OVL measurements at certain conditions. This correlation helps verify the accuracy of the optical measurement results and is applicable for the imaging base OVL method using several target types advance imaging metrology, advance imaging metrology in die OVL, and the scatterometrybase OVL method. Future plans include broadening the hybrid target design to better mimic each layer process conditions such as pattern density. Additionally, for memory devices we are developing hybrid targets which enable other methods of accuracy verification.
© *The Authors. Published by SPIE under a Creative Commons Attribution 3.0 Unported License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI.* [DOI: 10.1117/1.JMM.13.4.041404]

Keywords: overlay metrology; overlay; accuracy; device-correlated metrology; advance imaging metrology in die; advance imaging metrology; critical dimension scanning electron microscope.

Paper 14077SSP received Jun. 10, 2014; revised manuscript received Sep. 4, 2014; accepted for publication Sep. 4, 2014; published online Oct. 6, 2014.

1 Introduction

Overlay (OVL) continues to be one of the key challenges for lithography in semiconductor manufacturing, especially in light of the accelerated pace of device node shrinks, and the continuous delay in extreme ultraviolet lithography. According to the ITRS Roadmap in Fig. 1, the 20-nm node requires a 4-nm OVL for critical layers. This is a very tight OVL challenge by itself. Additionally, another OVL accuracy challenge is emerging due to the difference between the OVL of the metrology target versus the OVL of the actual device. There are several practical difficulties to achieve the exact same OVL for the device by measuring the OVL of an OVL target. One difficulty is that the current OVL measurement is performed on an OVL target, not on the actual device pattern. Since the design of the device pattern is different from previous generation OVL targets, the lithographic influence, e.g., image placement error and

nonlithographic influence such as etch bias, are not identical. Another difficulty is that the OVL measurement is performed after develop inspection (ADI) stage while the actual device OVL is determined at after etch inspection (AEI) or even later in the process. The OVL target environment is also different; usually the OVL target is located in the scribe-line whereas the device pattern is located inside the die. These differences have always existed, but a tight OVL margin requirement accelerates the potential yield damage if the mismatch is not accurately being controlled and accounted for.

2 DCM: Device-Correlated Metrology Concept

The inaccuracy mismatch between the OVL of the device and the OVL of the metrology target has been well known for a long time. Among the OVL accuracy methods outlined in Fig. 2, only methods #7 to 10 have excellent accuracy and they also allow correlation to the actual device OVL. These methods have already been implemented in the industry. For example, after device de-capping from the oxide protecting the previous layer, CD-SEM can directly

*Address all correspondence to: Tal Itzkovich, E-mail: Tal.Itzkovich@kla-tencor .com

Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
DRAM/ MPU/ ASIC (M1) ½ pitch (nm) (contacted)	52	45	40	36	32	28	25	23	20	18
DRAM CD control (3 sigma) (nm)	5.4	4.7	4.2	3.7	3.3	2.9	2.6	2.3	2.1	1.9
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23	20	18	16	14	13
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	54	45	38	32	27	24	21	19	17	15
Overlay (3 sigma) (nm)	10	9.0	8.0	7.1	6.4	5.7	5.1	4.5	4.0	3.6
Generic Pitch Splitting - Double Patterning Requirements Driven by MPU metal 1/2 Pitch										
Overlay 3s for MPU LFLE or LELE		5.5	4.6	3.8	3.1	2.6	2.3	2.0	1.8	1.5	1.4

Fig. 1 Overlay requirement in ITRS roadmap 2010 table. Marked in yellow are values that currently introduce with medium confidence, in red are values that currently introduce with low confidence. Cell color represents the performance rate of each method. Performances rate increase in the following order: orange-yellow-green-dark green.

	Method	Ease of data collection	Correlation to accuracy	Comments	Major use case
1	TMU			POR	All
2	Residuals		In most cases	POR	All
3	AEI-ADI	Need both ADI and AEI measurements	Etch bias might cause shifts	POR	All
4	Q-merit + ASC	Longer initial data collection	Improves accuracy due to asymmetry	New Algorithm	Only IBO for now
5	Different targets	Consumes space	Depends on targets	Rare	R&D
6	Programmed OVL & Linearity	Consumes space	Bias issues	Sensitivity check	R&D
7	CD-SEM targets	Need to add SEM AEI targets	Excellent to Device	DCM program	Most layers AEI. For DPL also ADI
8	Decap SEM	Destructive	Excellent to Device	AEI Cell matching	R&D
9	X-section TEM/SEM	Destructive	Excellent to Device	Can do ADI too	R&D
10	Electrical testing	Consumes space and resources	Excellent to Device	Used for R&D	R&D

Fig. 2 OVL accuracy methods benchmarking table. Cell color represents the performance rate of each method. Performances rate increase in the following order: orange-yellow-green-dark green. Marked in circle is the method which corresponds to DCM (OVL measurement using CD-SEM).

measure the actual device OVL. Another way is performing a cross section of the device and directly measuring the actual OVL with SEM or a transmission electron microscope. Electrical testing is also employed to calculate device test structures OVL from resistance measurements. The last three methods discussed in this table (methods 8 to 10) have limitations which mostly constrain them to the development phase or to a very low frequency use, and/or have a long info term. Among all the methods with excellent accuracy and device correlation, the only one which has high volume manufacturing (HVM) ease of use is utilizing CD-SEM OVL targets integrated into the optical targets. This is the method we recommend in this paper, and we refer to these targets as hybrid targets.

The DCM concept is reporting the actual device OVL considering both the measured OVL of the metrology target and the relative shift compared with actual device OVL. DCM basically has three main components. The first is to design the OVL target to have the same OVL behavior of the device pattern as much as possible. The second is measuring the OVL target correctly. If and when the first two components do not deliver enough accuracy, the third component comes to play. The third element is to accurately measure,

generate, and use a calibration map compensating the delta between the ADI of the optical OVL target and the actual OVL of the device at AEI. Thus, optical OVL measurement at the ADI can be used much in the same way as it is used today for the HVM environment. The correctable terms fed into the scanner take into account the calibration map to verify the device OVL is properly corrected.

2.1 DCM Design Rule Compatible Targets

The first DCM component is to design a target that will behave similarly to actual devices. Since pitch is one of the major factors for both lithographic and nonlithographic behaviors, we designed the OVL target elements to be segmented with a pitch below 400 nm, to make sure it is not resolved by the tool optical system. There is a balance between having a large pitch which is more process robust, especially in the scribe line areas where the process is less controlled, to the fine pitch of the device which allows the target to behave more like the device. The new designed targets are design rule compatible in more than 90% of their area. Design rule compatibility, especially with advanced nodes, in conjunction with small target size, allows placing the targets within the die itself. In die, the targets are
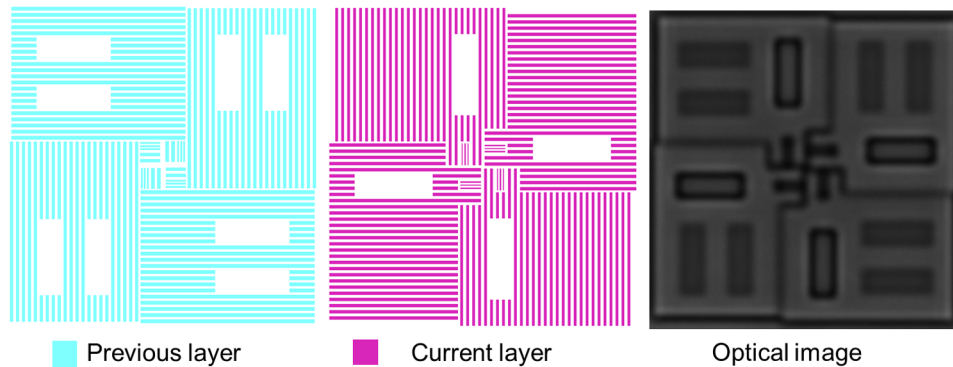
| Previous layer | Current layer | Optical image |

Fig. 3 Device-correlated metrology (DCM) target design example, from left to right: previous layer pattern graphic database system (GDS) layout, current layer pattern GDS layout, and optical image of the combined target.

obviously useful for high order corrections of the scanner. Once the target is compatible with the device design rules, it should also behave similarly to the device in response to the etch process. The target design shown in Fig. 3 has several improvements over previous generation AIMid targets. The high density pattern makes it self-protected and hence more robust to the polish process. To improve the correlation of the edge of the measured pattern with the pitch behavior, a subresolution assist feature and other optical proximity corrections can be applied to the design. The previous layer segmentation is perpendicular to the current layer segmentation to avoid the influence of one layer's signal on the other. One needs to take into account that target segmentation in most cases leads to lower light reflection and lower contrast, which can best be overcome with advanced metrology tools with more light output and sensitivity.

2.2 Accurate OVL Measurement

The second component of DCM is measuring the OVL target correctly. Even for the same OVL target, different OVL values can be reported by different measurement conditions or different targets.[1–6] For example, different color filter selection can report different OVL values, specifically when the OVL target exhibits asymmetry (for either current or previous layer). Therefore, measurement conditions which are defined in the measurement recipe need to be optimized to provide the correct OVL. The reader might want to refer to the elements of Fig. 2 in the following discussion. In the past, a low total measurement uncertainty (TMU) was one of the key elements for such selection, however, in advanced metrology tools, with a TMU performance below 0.5 nm, TMU is no longer a key indicator for accuracy or a component of inaccuracy. Model residuals are often used for determining the most accurate recipe or target. However, they also have systematic issues; for example, a measurement with a low sensitivity to OVL will produce low OVL values, potentially with low residuals. Another way to evaluate the accuracy is the Qmerit algorithm, described last year and this year in SPIE papers.[1–4] This algorithm produces a quantitative measure of the asymmetry impact. The Archer Self Calibration algorithm, described in a poster in this year's SPIE,[3] allows correcting for that asymmetry and improving the OVL accuracy. The OVL linearity arrays and programmed OVL shifts in different fields are used to verify the target sensitivity to

OVL and have some correlation to accuracy, but they are not immune to systematic OVL shifts. Another way to select the optimal recipe condition is by ADI to AEI matching, however, in some cases this is disturbed by an OVL bias introduced by the etch process. In this case and others, the CD-SEM target embedded in the hybrid target allows independent verification of the measurement accuracy. We can see in this table that all accuracy measurement methods with an HVM acceptable ease of use (methods 1 to 6) are not accurate enough. Using a CD-SEM hybrid target is both accurate and acceptable for HVM recipe verification. Obviously, during the development stage, the ease of use is less a factor and then different methods (methods 7 to 10) come into play. They will be discussed in the next section.

2.3 Calibration Map

The third component of DCM is to accurately measure, generate, and use a calibration map representing the delta between reference OVL measurement (at AEI) and OVL value of the OVL metrology target (at ADI). This calibration map can be used to calibrate the OVL before feeding the corrections to the scanner, so the scanner compensates for the difference and will print the device OVL more accurately on the next wafer. Reference OVL measurement can be done by CD-SEM result after de-cap, or an electrical test result or x-section result of the actual device, as captured in Fig. 2. These methods are commonly implemented at the development stage. The main disadvantages for these methods arise if the calibration map needs to be re-measured from time-to-time or when the process is changed. Re-measurement is required if stability issues are suspected, potentially resulting from process changes, metrology change and process or tool instability. Frequent re-measurement of the device OVL might result in significant effort and time delays, depending on the measurement method. Out of all the device correlation methods with excellent accuracy presented in this table, the one with the best ease of use is the insertion of CD-SEM targets in the hybrid OVL target, as introduced in this paper. In Fig. 3, such a CD-SEM target which resides in the center of the hybrid OVL target depicted in Fig. 3 can be seen. The CD-SEM image is superimposed on the schematic drawing of the OVL target. This type of CD-SEM target allows measuring the process induced effects (mostly litho and etch) that cause the shift between the target and

device-like elements on the same layer. We denote this shift as "ΔLayer1" for the delta between the target and device as measured by CD-SEM at the AEI of the previous layer. Also, similar to the current layer, we denote "ΔLayer2." These shifts, for both previous and current layers, can be introduced into a calibration map between the optical OVL measurement at ADI and the resulting device. Another element in the calibration map is obviously the difference between the optical AEI-ADI measurements. In the general case, the calibration map (Bias$_{Target-Device}$) will take the following form

$$Bias_{Target-device} = OVL_{Target(ADI)} - OVL_{Target(AEI)}$$
$$- \Delta Layer1 - \Delta Layer2. \qquad (1)$$

A simple example for using Eq. (1) is the following: a systematic constant 1-nm shift between the target and device at AEI on layer 1 (previous): ΔLayer1 = 3 nm. No shift at the current level at AEI ΔLayer2 = 0 nm. While ADI to AEI, the OVL bias as measured by the Archer is also a constant at OVL$_{Target(ADI)}$-OVL$_{Target(ADI)}$ = 2 nm in the opposite direction. The results of Eq. (1) will be 2-3-0 = −1 nm. Obviously, this should be done separately for X and Y directions. A more common case is when OVL$_{Target(ADI)}$-OVL$_{Target(ADI)}$ and also ΔLayer1/2 can be represented by a radial function of the distance from the center of the wafer (like an expansion or rotation term).

The method described in Eq. (1) is general and can be used for most layers. The optical OVL of the ADI and AEI can be measured in most cases. The AEI shift as measured by CD-SEM requires measuring both elements (target and device) at the same layer, without the need to penetrate any layer, and can be done relatively easily in HVM. The downside of using this method by itself is that it does not verify the accuracy of the optical measurement by independent means. Therefore, a need for independent validation of the optical OVL arises. This can be done for the OVL target at ADI only for a very few cases since CD-SEM normal conditions do not penetrate the resist and other layers below it. Though, for some double-patterning layer cases it can be done at ADI, when both the current and previous layers are at the same level. Such results were already published elsewhere.[7–10] A more common case is to validate by CD-SEM the OVL at the AEI. This can be done in many cases, such as when the etch process removes and reveals a conducting element of the previous layer. Depending on the process flow, in some cases this measurement can be done a few steps after AEI. Two kinds of OVL can be measured with CD-SEM at AEI: validation of the optical OVL target (measuring target elements) and validating the actual device OVL. In Fig. 4, a CD-SEM measurement of a DCM hybrid target is shown. This measurement allowed verification of the actual OVL values and measurement conditions for the relevant layers.

3 Results and Discussion

3.1 Results of Same Layer Shift: ΔLayer1 and ΔLayer2

Measurements of shift within the same layer done on the target seen in Figs. 3 and 5, resulted in significantly low values. This means that the segmentation chosen for the target does
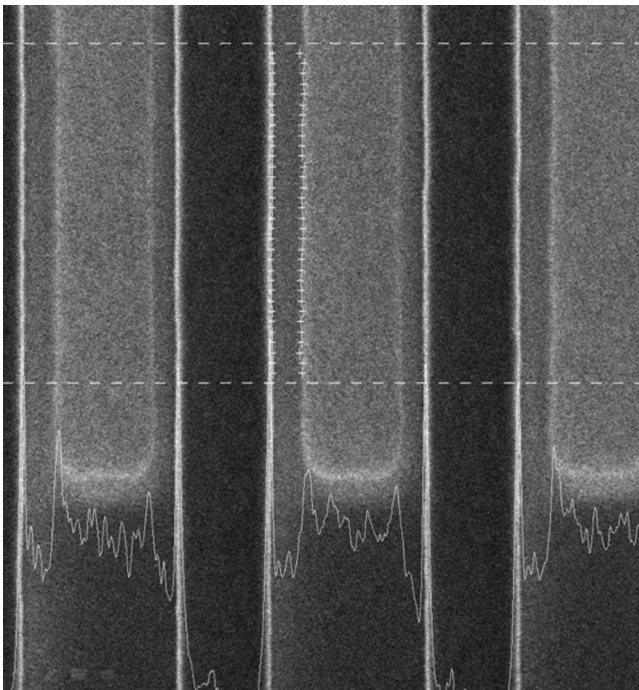

Fig. 4 Magnification of Hitachi CD-SEM measurement of an OVL CD-SEM target embedded within another DCM OVL target. The measurement was performed after AEI at a process step where both previous and current layers are visible and measurable by CD-SEM. In this picture OVL between poly and isolation layers was measured.
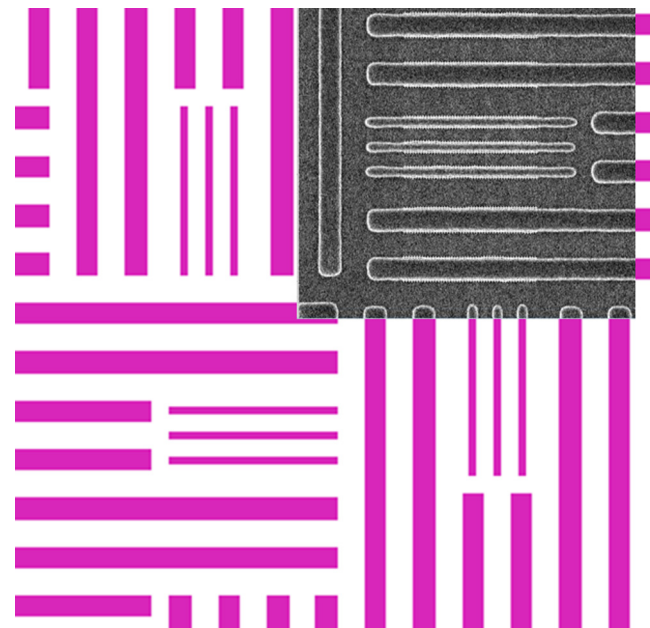

Fig. 5 Magnified image of the center area in the DCM target from image 3, both GDS layout and critical dimension scanning electron microscope (CD-SEM) image. Measuring the ΔLayer1 or ΔLayer2 values is done on this pattern at after etch inspection (AEI). ΔLayer1 or ΔLayer2 is the relative shift between target features (thick lines) and device features (thin lines). Note that this measurement is done by CD-SEM at each layer (previous and current) separately.
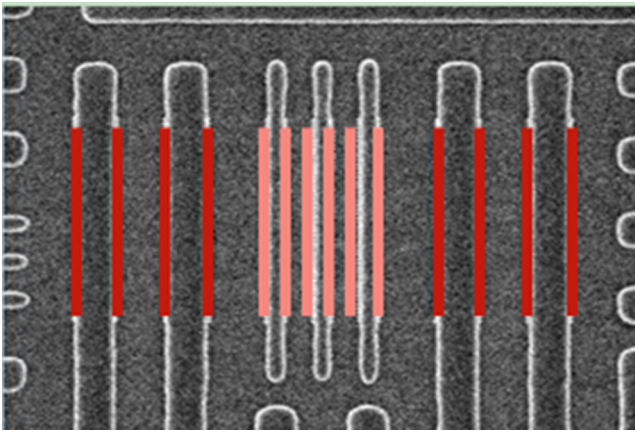
Fig. 6 Hitachi CD-SEM image of a CD-SEM target intended to measure the shift between the target and device at the same layer: ΔLayer1 and ΔLayer2. The red lines on the wider bars were used to determine the target's center. The pink lines on the thinner device like bars were used to determine the device's center.

not introduce significant systematic or other shifts between the target and the device. Note that this statement is dependent on the specific layer measured, the scanner and other process conditions, so it may vary case by case. In Fig. 6, the CD-SEM picture of the CD-SEM target is shown with the lines used for the OVL measurement. The pink lines on the thinner, device like bars were used to determine the device's center. The red lines on the wider bars were used to determine the target's center. The difference between the two centers as seen in Fig. 7 is mostly less than 0.5 nm in both X and Y directions. As can be seen in Fig. 8, the ΔLayer1 values measured at the four corners of each field do not show any wafer signature and are fairly constant. Since the shift is so small and does not exhibit a systematic wafer signature, we conclude that the shift is practically zero and is of the order of the CD-SEM measurement errors (0.2-nm reproducibility). In this case, Eq. (1) takes a simpler form as seen in Eq. (2)

$$\text{Bias}_{\text{Target}-\text{device}} = \text{OVL}_{\text{Target(ADI)}} - \text{OVL}_{\text{Target(AEI)}} - 0 - 0.$$

$$(2)$$

3.2 Results of Direct OVL Measurement with CD-SEM

As mentioned earlier, direct CD-SEM OVL measurements were used to verify which measurement conditions reflect
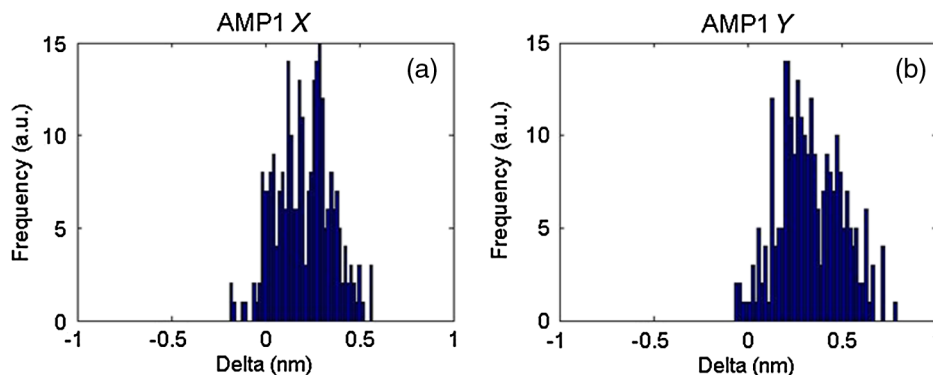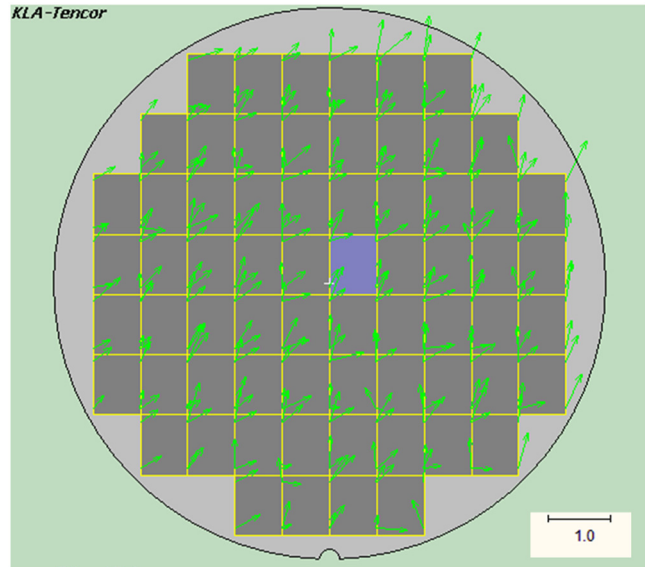

Fig. 8 ΔLayer1 element for the calibration map of the measurement described in Fig. 6 and shown in Fig. 7. CD-SEM has 0.2-nm reproducibility and in this experiment could measure a very small bias precisely without measurement error.
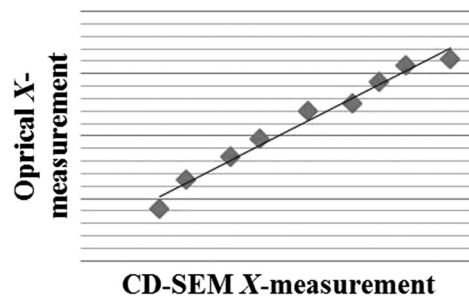

Fig. 9 Correlation between Archer 500 wide-near infrared color filter X-OVL and Hitachi CD-SEM direct X-OVL measurements done on the structure in Fig. 4. The slope is 1.07 over a range of a few nanometers and the R^2 is 0.98.

the most accurate OVL. When approaching the issue of verifying the optical OVL measurements, one needs to take into account that the CD-SEM has its own error budget. It also has specific best-known methods to calibrate it and improve the measurement accuracy. The co-operation with Hitachi was essential in those aspects. The optimized measurement

Fig. 7 Histogram of the measurement of ΔLayer1 described in Fig. 5 for both X and Y directions.

condition is the one which has sufficient measurement performance but must be accurate as well. In the results shown in Fig. 9, a good correlation is clear between the optical OVL measurements done with Archer500 using a wide near infrared (WNIR) color filter and the Hitachi CD-SEM measurements. The measurements were done on the Hybrid target depicted in Fig. 5 at AEI.

4 Summary

The metrology challenge described in this paper is that the OVL values did not correlate well with the electrical results for a specific OVL measurement. The relevant layer was found to have a challenging stack for optical OVL measurements. A study was conducted utilizing the DCM method. Hybrid process compatible OVL targets with embedded CD-SEM structures were designed and introduced into several layers.The first result showed that the same layer shift between the target and device is small and does not provide the root cause. Utilizing the CD-SEM direct OVL measurement, it was concluded that the Archer500 measurement using the WNIR color filter produced an accurate OVL measurement. Still, as a first measure, a calibration map was used to compensate for the bias between the process of record measurement and the accurate device OVL measurement. This method can be applied to other processes and layers where issues need to be solved. It can also be proactively introduced as a generic method to validate optical recipe OVL measurement accuracy and to generate calibration maps to resolve the target (ADI) to device (AEI) bias.

References

1. D. Kandel et al., "Overlay accuracy fundamentals," *Proc. SPIE* **8324**, 832417 (2012).
2. G. Cohen et al., "Overlay quality metric," *Proc. SPIE* **8324**, 832424 (2012).
3. E. Amit et al., "Overlay accuracy calibration," *Proc. SPIE* **8681**, 868184 (2013).
4. D. Klein et al., "Quality metric for accurate overlay control in <20 nm nodes," *Proc. SPIE* **8681**, 868187 (2013).
5. C. Chen and D. Choi, "Multi-level overlay techniques for improving DPL overlay control," *Proc. SPIE* **8324**, 83242A (2012).
6. C. Hwang and D. Choi, "Investigation on accuracy of process overlay measurement," *Proc. SPIE* **7971**, 79711F (2011).
7. S. Hotta et al., "Critical dimension scanning electron microscope local overlay measurement and its application for double patterning of complex shapes," *J. Micro/Nanolithogr. MEMS MOEMS* **10**(2), 023014 (2011).
8. S. Hotta et al., "Concerning the influence of pattern symmetry on CD-SEM local overlay measurements for double patterning of complex shapes," *Proc. SPIE* **7638**, 76381T (2010).
9. S. Hotta et al., "Critical dimension scanning electron microscope local overlay measurement and its application for double patterning of complex shapes," *J. Micro/Nanolithogr. MEMS MOEMS* **10**(2), 023014 (2011).
10. S. Halle et al., "Enhanced process control of pitch split double patterning by use of CD-SEM critical dimension uniformity and local overlay metrics," in *Proc. ASMC*, pp. 1–4 (2012).

Biographies of the authors are not available.