Study on various curvilinear data representations and their impact on mask and wafer manufacturing

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Abstract. Inverse lithography technology (ILT) optical proximity correction is going to play a critical role in addressing challenges of optical and EUV lithography as the industry pushes toward advanced nodes. One major barrier in adoption of ILT has been the mask writer's inability to efficiently write curvilinear patterns. With the introduction of multibeam mask writers, this barrier has been removed and widespread adoption of ILT is imminent. Traditionally, mask writers have accepted only trapezoidal inputs to the tool, though recent trends show that mask writers are adopting newer formats that already reduce file size. However, as the ILT shape complexity and data volume increases further for 5 nm nodes and beyond, the explosion of mask pattern data file size becomes a major concern. Therefore, there is a need for the industry to look toward other compact formats of data representation that will be capable of serving well for multiple generations of mask making. We compare various curvilinear data representation schemes and their value in the curvilinear ILT-based mask manufacturing flow. We demonstrate that given the nature of curvilinear data, representing it using native curve formats has significant value to reduce file size for future mask making flows. The same format may not be applicable for all types of features in the input mask. These options will be discussed. We will compare the value of such exotic representations with regular simplification approaches that reduce data volume using standard methods and discuss the extents and limits of all these techniques. To evaluate practical use of curvilinear representation in place of conventional piecewise linear representation, we manufacture and measure a photomask to evaluate the accuracy of curvilinear representations. Finally, we use EUV AIMS to assess the impact of curvilinear representation on wafer process window. © *The Authors. Published by SPIE under a Creative Commons Attribution 4.0 International License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI.* [DOI: 10.1117/1.JMM.20.4.041403]

1 Introduction

With the advent of multibeam mask writers, the use of ILT technology for wafer-level photolithography is now a real possibility.[1,2] ILT is a critical technology to improve the process window for advance nodes. Even though the ILT solutions across the industry are still evolving to achieve designs that can be manufactured with existing solutions, there is enough evidence already for the manufacturing industry to innovate and prepare to tackle the challenges in the manufacturing flow. The main challenge with ILT outputs is that they are curvilinear in nature.

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Curvilinear design is a big departure from conventional Manhattan and octangular designs. Manhattan designs have favorable properties that enable the EDA industry to develop extremely fast and robust software solutions that take advantage of these properties. Curvilinear designs put more stress on the classical algorithms used, and several exciting innovations in this domain are forthcoming. The other important challenge posed by the curvilinear designs is the explosion of file size. File size for both exchange of information between tools such as ILT optical proximity correction (OPC), mask process correction (MPC), and mask data preparation (MDP), and the mask writer is a cause for serious concern. A curvilinear polygon tends to have a larger footprint than a Manhattan polygon in most of the file formats. With increasing curvilinear data volume in ILT tools for 5 nm nodes and beyond, the explosion of file size in all stages of the manufacturing flow is a real problem that needs to be addressed soon.[3]

Huge files sizes put stress on many aspects of the IC manufacturing ecosystem. With file sizes for each layer being as much as several terabytes (TB), reliable storage and transfer is an obvious issue. The other main issue of large file sizes is that the downstream tools that read and process these files are at a disadvantage. The component of file reading (and writing) time in the downstream tools increases manifold due to their inherent serial and slow nature. Increased read/write time in software solutions in turn puts stress on the compute and storage cluster used by business units. Unless companies upgrade to more costly compute and storage clusters, they will struggle to maintain similar throughputs to the earlier Manhattan design processing flows. So even though file size seems like a shallow problem to solve, given that it is likely to put the entire ecosystem under stress, any improvement in file size is extremely crucial and worthy for investment by the industry today.

1.1 History and Value of Curvilinear OPC

The value of curved shapes over rectilinear shapes was illustrated by Fernandez Guasti in 1993[4] and Chris Mack in 2000[5] by comparing the diffraction images of square holes with varying degrees of corner roundness. As corner roundness increases the diffraction image transforms from a sinc function to a Bessel function. Comparing design data with the same area, the contrast and edge slope of a circular shape is improved over that of a square shape, affording up to 15% improvement in NILS and CD uniformity (Fig. 1).

Advances in OPC through the introduction of inverse lithography technology (ILT), which creates free-form shapes instead of rectilinear shapes, once again puts pressure on data volume and file size for which the industry would like new solutions. ILT OPC was introduced by Luminescent in 2006[6] as a method to achieve improved process window but requires curvilinear shapes (Fig. 2).

Effort was made to simplify the curvilinear mask shape (Fig. 3) but in 2009, Samsung and Luminescent demonstrated that the value of ILT was diminished with the level of simplification applied and that true curvilinear representation was important to extract the greatest value from ILT OPC (Fig. 4).[7]

OPC and MPC methods were developed that output curvilinear shapes approximated by piecewise linear polygons where accuracy and data volume is determined by the number of
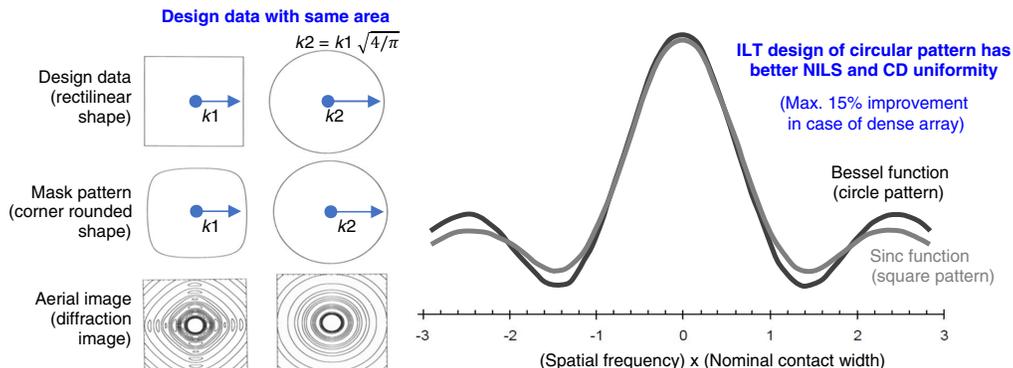
Fig. 1 Imaging comparison of squares and circles.
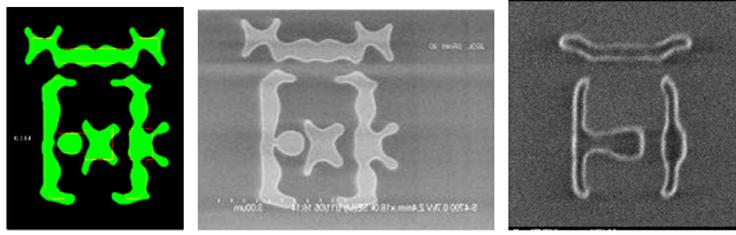
Fig. 2 Luminescent curvilinear design, mask, and wafer shapes.

Raw contoured ILT mask — C0 — C1 — C2 — C3 — C4
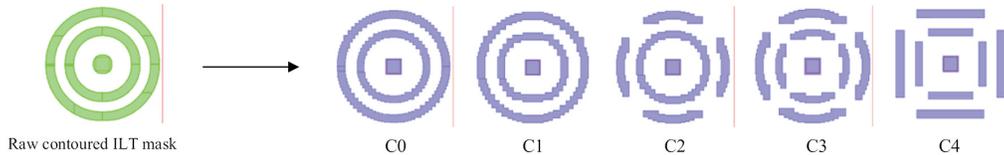
Fig. 3 Test layouts to evaluate mask simplification impact on write time and wafer process window.
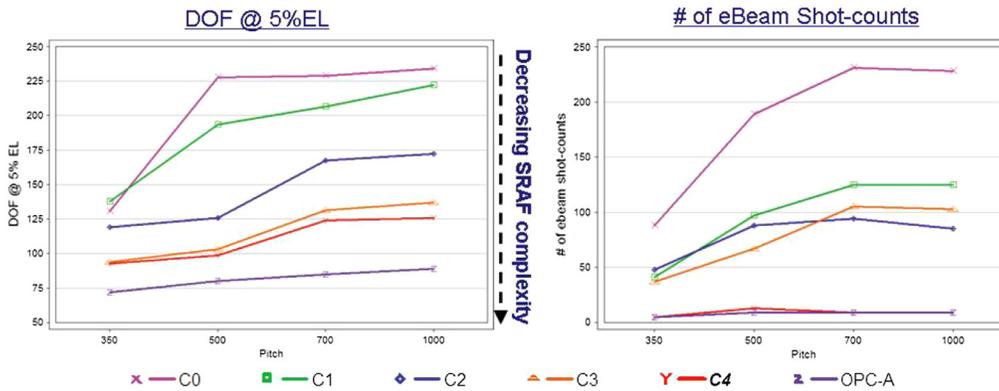
Fig. 4 Wafer depth of focus and mask writer shot count as a function of curvilinear OPC simplification.

vertices used to define each polygon. However, the general use of curvilinear shapes could not be immediately realized with the existing variable shaped beam (VSB) mask writers, which construct patterns on the mask from discrete exposures of rectangles and right triangles. Since VSB write time is directly related to pattern complexity, VSB write time for curvilinear mask patterns was generally unacceptable to achieve reasonable mask cost and cycle times. However, the recent introduction of multibeam mask writers (MBMW)[8] where raster scan methods enable write time independent of data complexity have now made ILT OPC, and the resulting curvilinear mask shapes a practical reality, which drives the urgency for a data volume solution.

1.2 *Current Status of Curvilinear and MBMW*

Mask manufacturing represents the first physical manifestation of design intent. The design is rendered for mask manufacturing including scaling, MPC, sizing, rotation, mirroring, placement in the mask layout, fracturing to a mask exposure tool writer) format, and finally exposed in resist on the mask. The format in which the data are delivered to mask manufacturing is important to the efficiency of data transfer, data manipulation, and mask writing itself. Critical masks have largely been manufactured using electron beam (e-beam) writing technology. Several kinds of mask writers have been proposed and developed. While many approaches to e-beam lithography have been proposed,[9] the dominant technology used in production for the last 30 years has
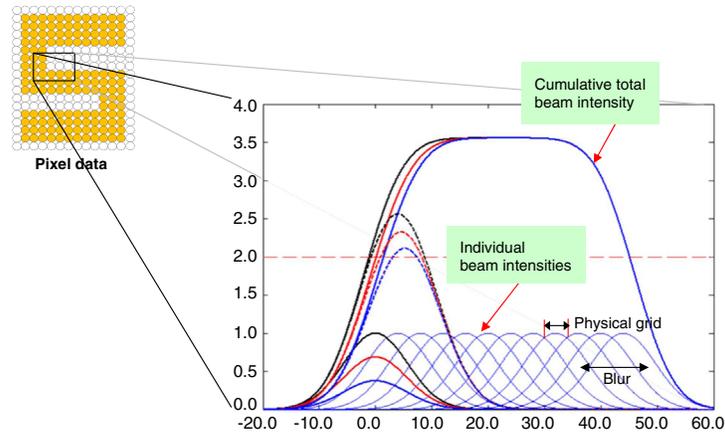
Fig. 5 Illustration of multibeam raster scan gray-scale writing strategy.

been VSB. Write time for VSB is a direct function of the number of exposure "shots" required to compose the mask pattern, which means that write time becomes longer with increasing mask pattern complexity. VSB writer manufacturers have successfully been able to keep up with increasing mask pattern complexity by increasing beam current, which reduces the per shot exposure time and by reducing system overhead times. However, the data volume explosion due to the increase in curvilinear OPC methods has caused VSB writers to have reached their practical limits and have given rise to multi-beam technology. MBMW make use of raster scan exposure strategies to achieve exposure rate independent of data complexity and multibeam parallelism to achieve high areal exposure rate combined with high precision edge placement (Fig. 5). Raster scan mask writing was introduced by the AT&T Bell Labs EBES tool,[10] which was successfully commercialized by ETEC.[11] Multibeam mask exposure was introduced by ATEQ [12] with linear arrays of 8 or 32 beams for use with laser exposure systems. Two-dimensional exposure element arrays were introduced by Micronic with their spatial light modulator technology.[13] IMS and NuFlare[14] have both solved how to create two-dimensional arrays of electron beam-lets to enable massively parallel e-beam exposure systems. Due to the high rate of exposure, the high precision made possible by the MEMs technology used to manufacture the aperture arrays, and the independence of write time to pattern complexity, these modern mask writers are well-suited to enable the practical use of curvilinear OPC methods (Fig. 6). Mask
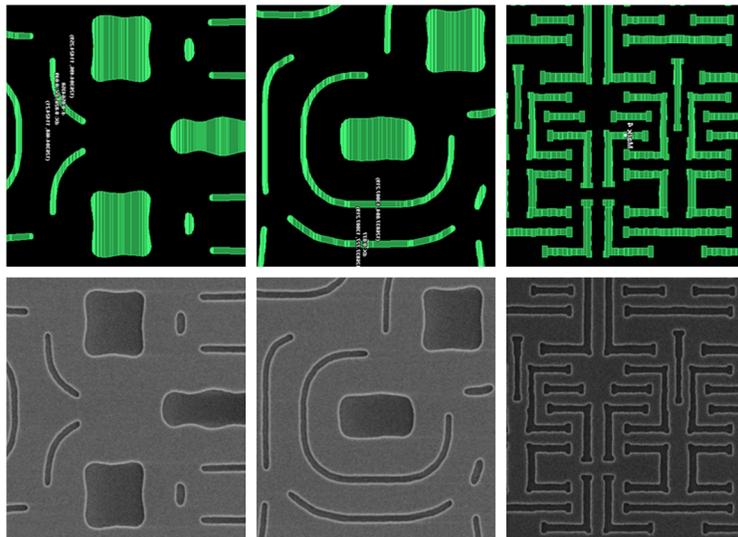
Fig. 6 Examples of curvilinear mask layouts and corresponding mask SEM images written with MBMW.
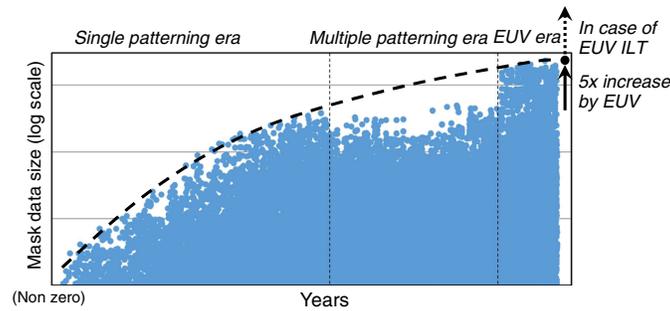
Fig. 7 Mask data volume over time at Samsung, illustrating the impact of single and multipatterning eras and the increases caused by EUV and anticipated by curvilinear OPC.

complexity has grown significantly over time as shown in Fig. 7, which compiles mask data volume at Samsung from the single patterning era, where there was a strong relationship between data volume per mask versus time due to the continuing miniaturization and increase in density driven by Moore's law, through the multipatterning era where the increase in mask volume increased but data volume per mask was limited by k1 at 193 nm exposure wavelength to the continuation of data volume ramp per mask with the introduction of single patterned EUV. The increase in data volume per mask for EUV compared to DUV multipatterning is observed to be 5× with an even greater increase anticipated with the introduction of EUV curvilinear OPC.

1.3 *Implementation Challenges of Curvilinear Layouts*

The SEMI standard P39 OASIS (Open Artwork System Interchange Standard) is the dominant format used to describe integrated circuit physical layouts.[15–17] Curvilinear intent is approximated in P39 using piecewise linear representation to form polygons. The number of edges used to represent the curvilinear intent is optimally determined by the accuracy required by downstream processes. Too many edges increase data volume and execution time (e.g., OPC, MPC, fracture), but too few edges reduce accuracy. Tools that create curvilinear output are not necessarily aware (today, at least) of the downstream requirements so it is easy to produce more edges than are necessary. Mask lithography and process capability limit the resolvable jog size and resolvable convex and concave corner radii. Tools upstream from mask data prep need to recognize and adhere to mask MRC rules and MRC validation needs to consider these limits. Data operations can introduce jogs and discontinuities in curvilinear representation. While the intent of a jog in rectilinear data is often evident, this is not always the case in curvilinear data. The intent needs to be interpreted—are the jogs intended or spurious? EDA tools are optimized for Manhattan and 45-deg edges. Operations such as sizing, Boolean transformations, and metrology need to be enhanced for skew edges. Ultimately the mask writer, die to database (D2DB) mask inspection tools and mask repair tools need to consume curvilinear data and rasterize. These tools need to consume and operate on curvilinear data efficiently. If tool-specific fracture formats are required, they must not lose curvilinear intent or create data volume-related bottlenecks. Alternative forms to represent curvilinear data such as polynomial or spline-based approaches need to be either natively supported or transformations to and from curvilinear to piecewise linear need to be lossless. Finally, the industry needs to agree to support any new curvilinear constructs proposed.

2 Evaluation of Curvilinear Layout Approaches

2.1 *Overview of Potential Solutions*

2.1.1 *Polygon simplification*

Several classical polygon simplification techniques and their variants are available in MDP tools. One of the important ones that suits curvilinear designs is based on traditional polygon
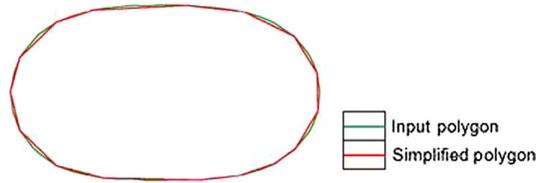
Fig. 8 Polygon simplification.

simplification known as the Visvalingam–Whyatt algorithm.[18] This algorithm reduces vertices in polygons based on a specified area change criterion. However, the area criterion on its own is not a sufficient constraint, as it can lead to removal of multiple consecutive vertices; each changes only a small amount of area, but cumulative area change could be far more. Also, without specifying the amount of deviation allowed, the area criterion can lead to large deviations at critical regions of polygons, leading to image fidelity issues. Therefore, deviation criterion along with cumulative area change criterion was added on top of classic Visvalingam-Whyatt approach. Figure 8 shows an example of polygon simplification. Simplified polygon will always be smaller than original for convex regions as seen in this example and bigger for concave regions, so the overall area change will still be large.

2.1.2 *Piecewise Bezier representation*

Bezier curves are defined using Bernstein polynomial basis.[19] Quadratic Bezier curves are used, which are defined by three control points (control polygon) and dictate shape of the curve:

$$B(t) = \sum_{i=0}^{n} \binom{n}{i} (1-t)^{n-i} t^i \mathbf{P}_i \quad B(t) = (1-t)^2 \mathbf{P_0} + 2(1-t)t\mathbf{P_1} + t^2\mathbf{P_2}, \quad 0 <= t <= 1.$$

A curvilinear polygon is represented with piecewise Bezier curve in EDA tools, i.e., a series of quadratic Bezier curves joined end to end. Conversion from piecewise linear representation to piecewise Bezier representation is done adhering to the specified deviation tolerance. As shown in Fig. 9, the input curvilinear polygon can be compactly represented by six quadratic Bezier curves joined end to end such that their control points form a closed polygon. A utility to convert Bezier representation back to piecewise linear representation was implemented to compare output to input by sampling the Bezier curve over a specified parameter interval. This sampled output is used to evaluate the impact of Bezier curve fitting on mask and wafer images in Sec. 6.

2.1.3 *B-spline representation*

A B-spline curve is a piecewise polynomial curve that smoothly transitions from subinterval to subinterval. A knot vector must be specified, which determines the values of parameter t at which the pieces of polynomial curve join:[20]

$$B(t) = \sum_{i=0}^{n} N_{i,k}(t)\mathbf{P_i} \quad \begin{aligned} N_{t,1}(t) &= \begin{cases} 1, & t_i \leq t < t_{i+1} \\ 0, & \text{otherwise} \end{cases} \\ N_{t,k}(t) &= \frac{t-t_i}{t_{i+k-1}-t_i} N_{i,k-1}(t) + \frac{t_{i+k}-t}{t_{i+k}-t_{i+1}} N_{i+1,k-1}(t) \end{aligned}.$$
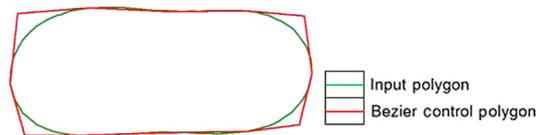
Fig. 9 Piecewise Bezier representation.
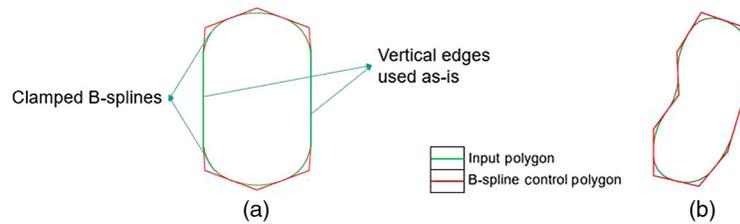
Fig. 10 B-spline representation: (a) clamped B-spline and (b) unclamped B-spline.

Again, just like piecewise Bezier, conversion to B-spline is also done subject to the specified deviation criterion. Two types of quadratic B-spline curves were evaluated:

- **Clamped B-spline curves:** B-spline curves that pass through first and last control points are considered as clamped. To achieve the clamped effect with quadratic B-splines, the first three and last three knots of the knot vector are repeated. Clamped B-splines are helpful when only certain portion of a polygon needs to represented with curves, and rest in piecewise linear form. Figure 10(a) shows clamped B-spline example where curved portions at top and bottom of the polygon are represented using clamped B-splines and long vertical edges are retained as is.
- **Unclamped B-spline curves:** Unclamped B-spline curves do not pass through control points. Quadratic unclamped B-splines can be used to represent a closed curve by wrapping last two control points around first two control points with a uniform knot vector. Figure 10(b) shows an unclamped B-spline curve being used to represent a closed polygon.

2.1.4 *Curvature-based fragmentation*

The last approach we are calling curvature-based fragmentation, or "CBF." The CBF approach attempts to co-optimize file size, accuracy, and MPC execution time. One factor that affects MPC time is the number of fragments that need to be moved. The optimum fragment length is related to the local curvature and the overall mask process blur. High acuity mask processes with high curvature corners require smaller fragments while low acuity mask processes and gentle curves or straight edges can be accurately represented by longer fragments. Therefore, CBF generates shorter edges at high curvature regions and longer edges at low curvature regions (Fig. 11). Similar to the other methods described, an error tolerance can be specified to further tune the output characteristics. Note that the degree of file size compaction achieved depends to some extent on the ability of the OPC tool to produce optimal output.

2.1.5 *Path polygons*

Path polygons are defined by their skeleton or centerline, with a constant width along the skeleton and same width semicircles at the ends. ILT tools can take advantage of such a feature and strive to generate such SRAFs whose width is constant everywhere and ends are also
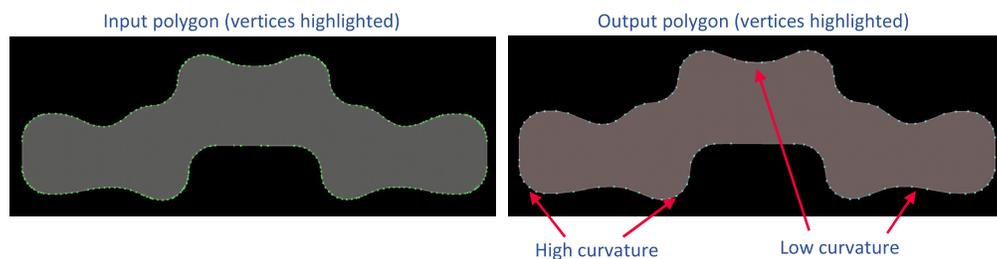
Fig. 11 Curvilinear-based fragmentation example.
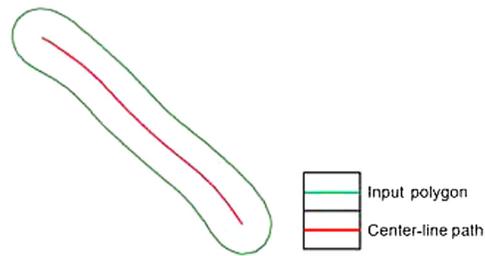
Fig. 12 Path polygon representation.

semicircular of the same radius. The actual centerline can even be converted to curve representation such as Bezier or B-spline to further boost the compaction. Figure 12 shows path polygon or center-line-based representation of curvilinear SRAF. The original pattern can be retrieved by expanding the centerline on each side by the width value and placing the same width radius semicircles at the ends.

2.2 Conversion Using Deviation Tolerance

Curvilinear data are defined using piecewise linear polygons (sequence of line segments) traditionally. All the curvilinear data representations discussed in this paper do not retain the input piecewise linear polygon description as-is. They all convert the description to other forms which are lossy in nature and cannot generate back the original input polygon exactly. However, the exact replication of input polygons is not a very important requirement as the input edges that form the piecewise curvilinear polygons are themselves not sacrosanct. These edges are generally formed after processing a mask image within the ILT designs and the location, length, and the end coordinates of the edges themselves are not very important. As long as the curve of the feature is well placed in the necessary location, it does not matter how and where the line segments are located. Hence, while converting from piecewise linear form to other forms, in our opinion it is acceptable to convert such that the curve location is still in the necessary location, but the edges need not be the same. However, this claim can only be verified using various mask quality checks employed in the field—OPC and MPC verification, mask, wafer inspections, etc. Some results of these quality checks are discussed in Sec. 6.

All the techniques presented work with a deviation tolerance parameter. Deviation tolerance is the amount of tolerance from the original curvilinear polygon allowed, to generate a more compact representation. Deviation is defined as the maximum perpendicular distance ($L1$-norm) between the input polygon and the output representation. Obviously, the higher the deviation value, the higher the compaction will be. Deviation from 0.1 to 2 nm were tried in this work. Figure 13 shows a simple example of two equivalent curvilinear polygons for a given deviation value.
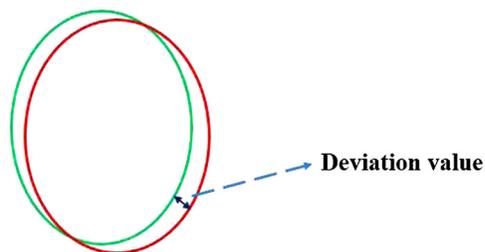
Fig. 13 Illustration of deviation between two curvilinear figures: the maximum distance between the two figures.

3 Experimental Setup

3.1 *User Defined Records in SEMI P39 OASIS*

SEMI P39 is the industry standard exchange format to generate output of tools such as ILT OPC and MPC. Some of the salient features of this format are also adopted by some mask writer formats. P39 has several characteristics that enable EDA tools generate extremely compact data for Manhattan and octangular designs. Even for curvilinear designs, the amount of compaction that P39 achieves is significant.

Hence, it makes sense to compare the data size reduction of the new representations with the same data in regular P39 format. Along with standard record types covering all facets of IC data composition, P39 has an extension record type that lets users write polygon data in their own format. Most of our data representations, discussed in further sections, used this user-defined record type to generate P39 output. By doing so, the assessment of file size changes became trivial; original and user-defined P39 files had to be simply compared.

3.2 *Format Used*

Polygon simplification (Sec. 2.1.1) and curvature-based fragmentation (Sec. 2.1.4) output was again piecewise linear polygon format and hence did not need to use the user-defined record type of P39.

Bezier (Sec. 2.1.2) and B-spline (Sec. 2.1.3) are curve formats with no equivalent record types in P39. Hence, these were stored in the user-defined records of P39. Following information is stored for curve formats:

- Curve format type (Bezier/clamped B-spline/unclamped B-spline)
- Number of control points in curve control polygon.
- Control points coordinates.
- If any section of polygon needs to be retained as is, information about retained piecewise linear section is stored.

P39 format has a provision for storing path polygons, which are defined by a sequence of line segments. A width for these line segments should also be specified. However, the format does not allow for a rounded, semicircular start and end for this path. Interestingly, the older GDSII format allowed for such rounded corners for path polygons. In our work, we have assumed that the P39 format can be revised to allow for rounded path polygons, just as done in the GDSII format. This feature was used to write the path polygons as shown in Sec. 2.1.5.

4 Compaction Results

4.1 *Vertex Count Reduction*

Vertex count reduction is an important evaluation criterion for compaction techniques described in Sec. 2.1. Here, the vertex count of piecewise linear representation is compared with vertex count of compact representations. For polygon simplification, the vertex count of simplified polygon is used. For piecewise Bezier and B-spline representations, the vertex count of control polygon is used and for path polygon, vertex count of center-line is used for comparison. Different set of test cases with constant width polygons were used to evaluate path polygon approach. Figure 14 shows the results of this comparison. Test cases with complex curvilinear patterns and high vertex count show most reduction especially with curve formats. Best average compaction (6.5×) is observed with Beziers for 1-nm deviation tolerance, closely followed by other representations. It should be noted that since this is a compilation of several studies, and due to time and resource constraints, not all compaction methods received exactly the same evaluation.
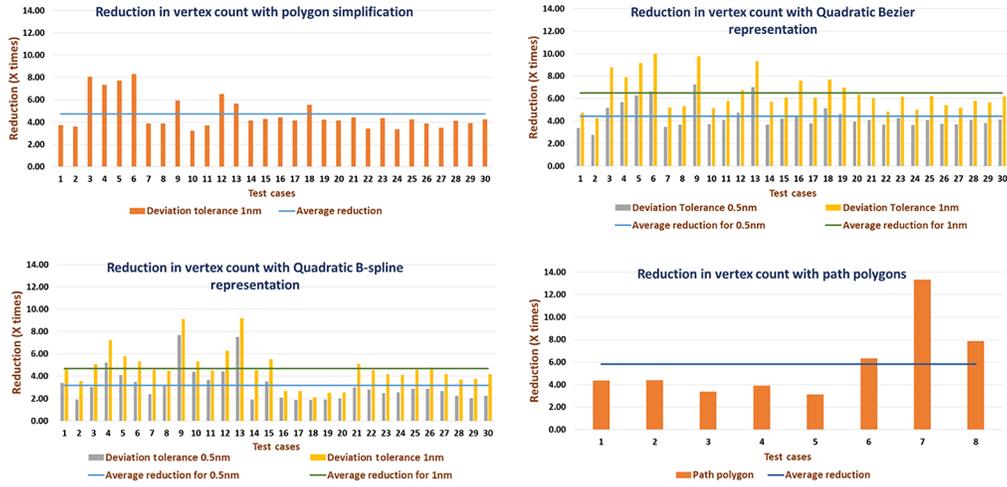
Fig. 14 Vertex count reduction results.
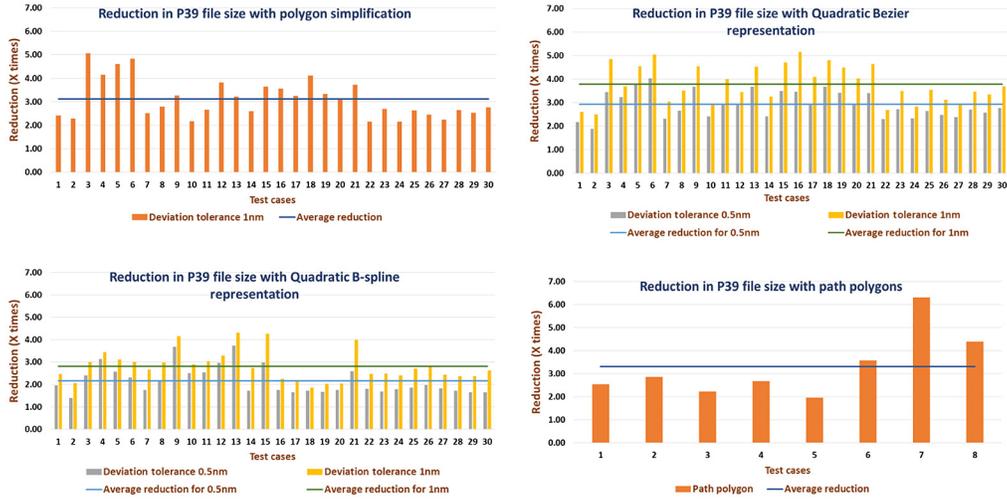
Fig. 15 P39 file size reduction results.

4.2 *P39 File Size Reduction*

For file size reduction, original P39 files are compared with P39 files written using compact representations. Figure 15 shows this comparison. Again, Bezier representations have best average file size reduction (3.8×) for 1-nm deviation tolerance. Note that file size reduction obtained is not as high as vertex count reduction due to good compaction features of P39. Compaction for curve formats can be further improved by improving curve description strategies.

4.3 *Change with Varying Precisions*

With ILT designs moving to higher precision, it is interesting to check file size reduction at higher precision. Our experiments show that file size reduction improves for higher precision. Figure 16 shows file size reduction with B-spline representation for the same set of curvilinear layouts at 0.1 and 0.01 nm precision. Results at 0.01-nm precision are quite promising with improved average compaction and some test cases showing 6× to 7× compaction. Similar file size reduction trend is observed with other representations as well.
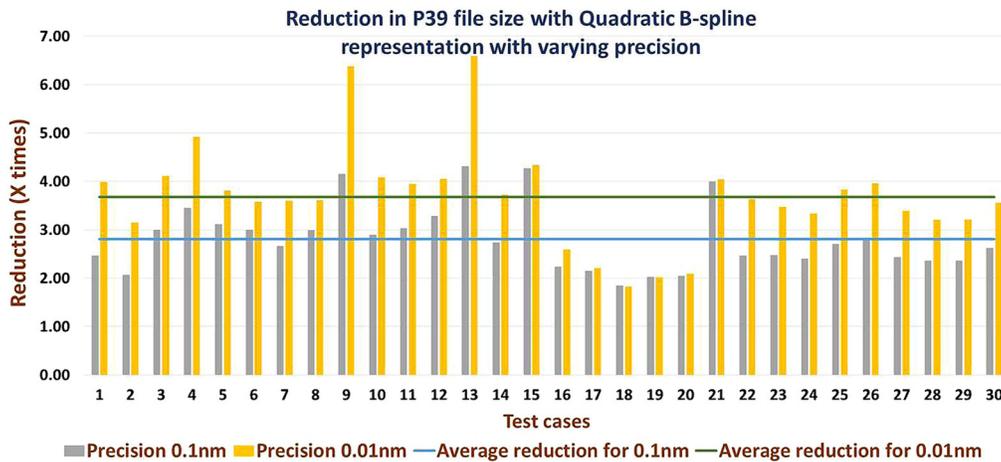
Fig. 16 Change with varying precisions with B-spline representation.

Table 1 Matrix of compaction technique, magnification, and error tolerance used to produce output for evaluation.

Compaction technique	Magnifications	Error criteria used
Bezier curve fitting	All	0.1, 0.5, 1, 2 nm
B-Spline curve fitting	2×	0.5, 1, 2 nm
Polygon simplification	All	0.1, 0.5, 1, 2 nm
Curvature-based fragmentation	2×, 4×, 6×	1 nm

5 Mask Verification

Fourteen curvilinear test layouts were provided by Samsung, derived from advanced logic and DRAM device layers. Siemens converted these to magnified files at different scale factors to explore compaction value as a function of pattern scale. Using the methods described earlier, all four compaction methods were applied and output at various error tolerances (Table 1). An EUV mask was manufactured by Samsung, mask CDs and SEM images from six of the layouts (shown in Fig. 17) were sampled, and contours were extracted from the SEM images. Typical dimensions from the sampled images ranged from 50 to 350 nm at 4× mask scale.

5.1 Results

Figures 18 and 19 summarize the reduction factors achieved for each of the 14 patterns at three error tolerances using the Bezier and B-spline compaction approaches. Compaction varies with

Dumbbell	Rectangle with ears	Rectangle with rounded corners	Wiggle 01	Wiggle 03	SRAF
0.05 ~ 0.35μm	0.3μm	0.05 ~ 0.1μm	0.05 ~ 0.1μm	~0.05μm	0.02~0.16μm
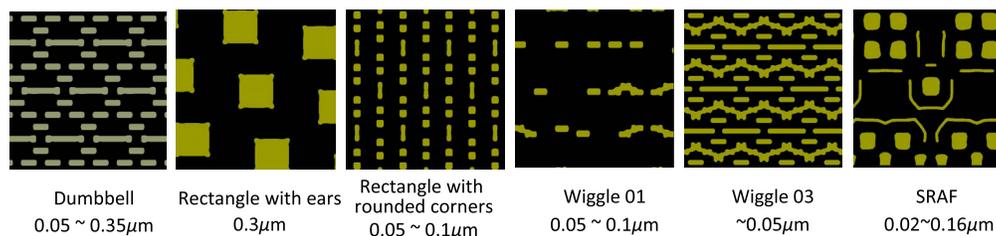
Fig. 17 Test patterns evaluated with four curvilinear compaction approaches.
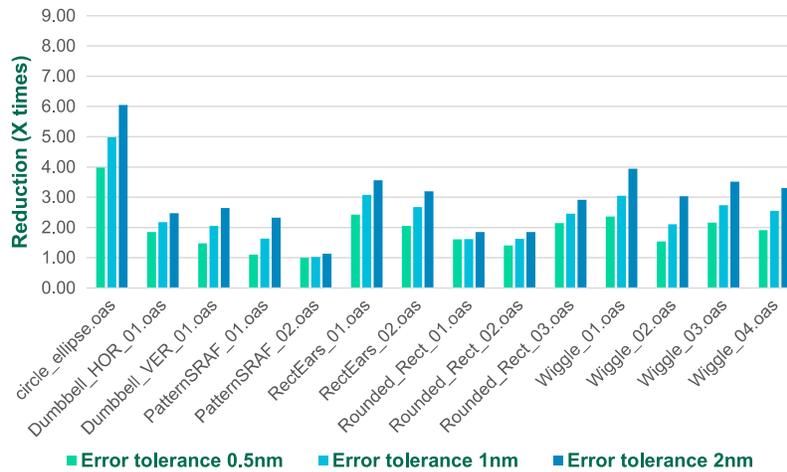
Fig. 18 Reduction in OASIS file size with quadratic B-spline representation in XGEOMETRY records.
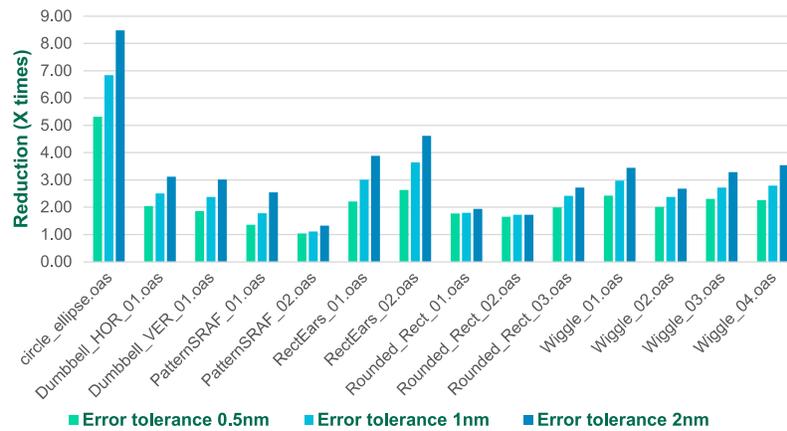
Fig. 19 Reduction in OASIS file size with quadratic Bezier representation in XGEOMETRY records.

pattern shape and complexity with almost no compaction for some patterns and up to 6× for B-spline and up to 8× for Bezier, depending on the error tolerance specified.

Figure 20 shows compaction results for the curvature-based fragmentation approach for two different pattern scale factors. As expected, larger patterns do not achieve the same level of compaction. Simply, scaling the fragment sizes is not possible since the minimum required fragment size is dependent on the mask model. However, compaction of 2× to 3× is demonstrated for typical advanced node layout pattern sizes. Practical benefits of CBF include immediate availability since no new format is required as well as the potential to minimize MPC execution time.

Summarizing the file compaction results (Fig. 21), on average, Bezier and B-spline provide the greatest opportunity for file size reduction especially at larger error tolerances. At 1-nm error tolerance, average compaction ranges from 1.99× for CBF to 2.72× for Bezier. CBF fragmentation is based on the MPC model. Smaller fragments do not improve accuracy but increase data volume and MPC execution time. Larger fragments can reduce data volume and MPC execution time but at the potential expense of accuracy. Both Bezier and B-spline methods require changes to the layout data format and conversion to polygons to use conventional data processing code as well as mask manufacturing. Over time it is conceivable that OPC, MPC, fracture, and mask writer software could change to directly use Bezier/B-spline representation. General and MPC-specific (CBF) polygon simplification methods have the immediate advantage of not requiring
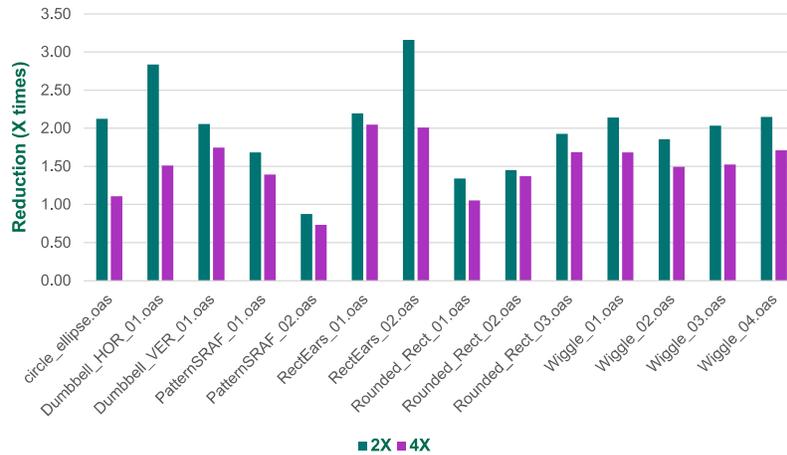
Fig. 20 Reduction in OASIS file size with curvature-based fragmentation.
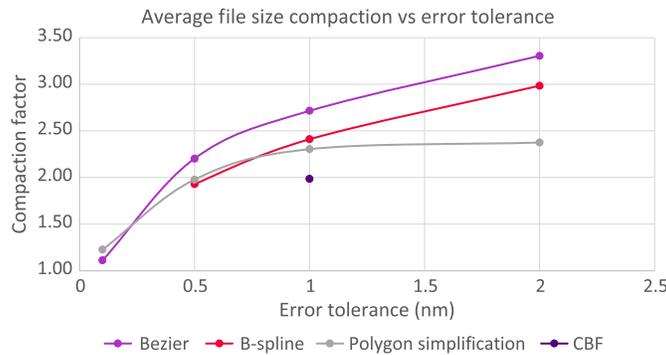
Fig. 21 Summary of file compaction results for four different approaches as a function of error tolerance.

new format introduction but have more modest compaction results. General polygon simplification techniques such as Visvalingam–Wyatt tend to make convex regions smaller and concave regions larger resulting in mean CD shifts. Certain layout shapes, such as ellipses, achieve significantly higher compaction with Bezier or B-spline approaches.

All patterns were converted to all four types of curvilinear representation and exposed with the IMS MBMW. Contours were extracted from SEM images of the mask patterns (Fig. 22) and output as GDS layers. Critical dimension (CD) measurements were made from the contours and compared with CD measurements from reference patterns written without curvilinear compaction. CD average and RMS edge position error were calculated and normalized to the original input pattern CD statistics.

Six of the 14 test layouts printed on the mask with 12 combinations of curvilinear representation and fitting error tolerance were evaluated for CD control. EPE average (Fig. 23) and

Dumbbell	Rectangle with ears	Rectangle with rounded corners	Wiggle 01	Wiggle 03	SRAF
0.05 ~ 0.35μm	0.3μm	0.05 ~ 0.1μm	0.05 ~ 0.1μm	~0.05μm	0.02~0.16μm
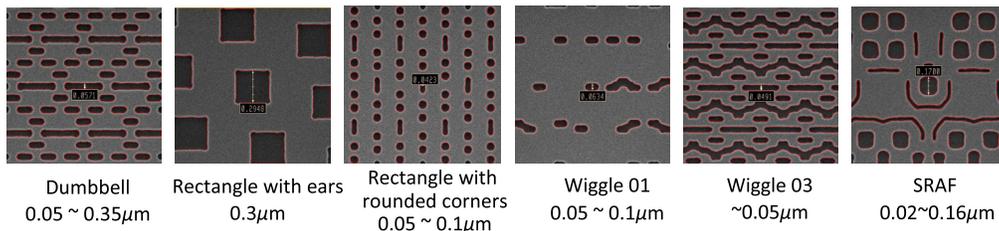
Fig. 22 Contours (in red) used for metrology shown overlaid on mask SEM images.
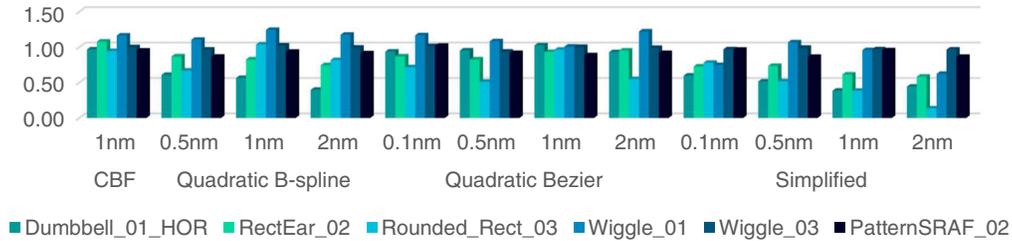
Fig. 23 EPE average relative to reference as measured on the mask.
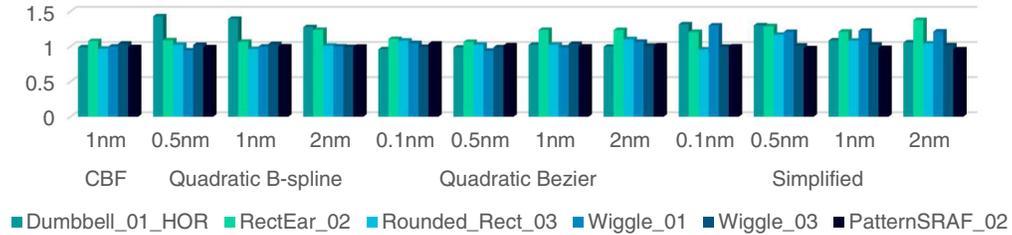
Fig. 24 EPE RMS relative to reference as measured on the mask.

RMS (Fig. 24) are shown here, normalized by the values from the reference layouts. Despite some sensitivity to specific pattern layouts, all formats are comparable to the reference layouts in terms of patterning accuracy.

To more clearly compare the four curvilinear approaches and understand the impact of fitting error tolerance, the results were averaged across all size layouts evaluated (Table 2). All approaches show similar average and RMS EPE increase compared with the baseline. Error tolerance does not significantly impact EPE within the range tested and for this mask process. The additional compaction afforded by Bezier and B-spline could be achievable without sacrificing accuracy. Validation of wafer process window is desirable to narrow the approaches and determine allowable error tolerance.

Implementing new curvilinear formats needs to be introduced incrementally. Here, we review three flows that represent one approach to consider. In flow 1 (Fig. 25), OPC produces CBF that is OPC-verified. MPC can use the OPC output directly as the MPC target—no unverified conversion step is required. MPC writes CBF, which maintains CBF compaction advantages to the writer. No writer or format changes are required.

Flow 2 (Fig. 26) is the same as flow 1 except that MPC outputs B-spline fracture data. Again, no change to P39 required; however, the fracture format and mask writer need to support B-spline.

Table 2 Summary of compaction, average EPE and RMS EME as a function of compaction approach and error tolerance applied during compaction.

		Compaction (nX)				AFG EPE (nX) to baseline				RMS EPE (nX) to baseline			
		Polygon				Polygon				Polygon			
		Bezier	B-spline	Simplify	CBF	Bezier	B-spline	Simplify	CBF	Bezier	B-spline	Simplify	CBF
Error tolerance	0.1 nm	1.1	—	1.2	—	1.0	—	0.8	—	1.0	—	1.1	—
	0.5 nm	2.2	1.9	2.0	—	0.9	0.9	0.8	—	1.0	1.1	1.2	—
	1.0 nm	2.7	2.4	2.3	2.0	1.0	0.9	0.7	1.0	1.1	1.1	1.1	1.0
	2.0 nm	3.3	3.0	2.4	—	0.9	0.8	0.6	—	1.1	1.1	1.1	—
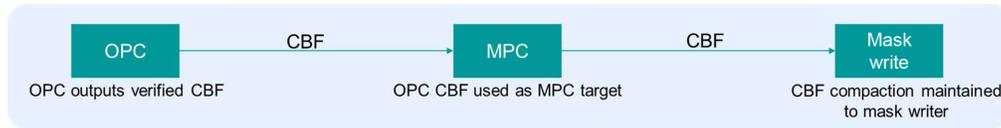
Fig. 25 Flow 1: CBF is introduced as exchange format from OPC to mask write.
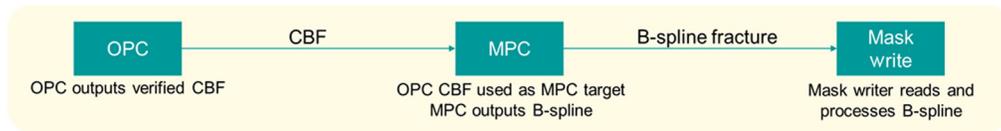
Fig. 26 Flow 2: B-spline introduced between MPC and mask write.
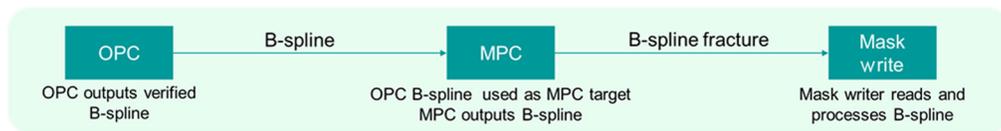
Fig. 27 Flow 3: complete flow supports B-spline.

In flow 3 (Fig. 27), OPC outputs verified B-spline, gaining compaction value over CBF. MPC reads and writes B-spline. Enhancements to P39 are required to implement this flow and gain the greatest compaction value.

6 Wafer Verification

We measured the mask patterns by EUV AIMS tool, as shown in Fig 28. To analyze the pattern fidelity, we subtracted the aerial images of mask patterns with respect to aerial images of reference pattern, that is, (results of compacted design) – (results of noncompacted design). We chose the most challenging pattern to observe the difference enhancement by tolerance clearly. In Fig. 29, "pattern with SRAF," which is the sixth pattern of Fig. 28, shows the difference of aerial image from the baseline. By comparison of EPE measurements, quadratic Bezier of 0.1 nm tolerance and quadratic Bezier of 2 nm have similar RMS error. However, aerial images clearly show the quadratic Bezier of 0.1 nm tolerance has 50% smaller error than quadratic Bezier of 2 nm. According to EUV AIMS measurement, we concluded quadratic Bezier of 2 nm is unacceptable as a solution of pattern compaction. Based on this result, the aerial image analysis rather than SEM EPE measurement is necessary method for verification of pattern compaction.

| Dumbbell | Rectangle with ears | Rectangle with rounded corners | Wiggle01 | Wiggle03 | SRAF |
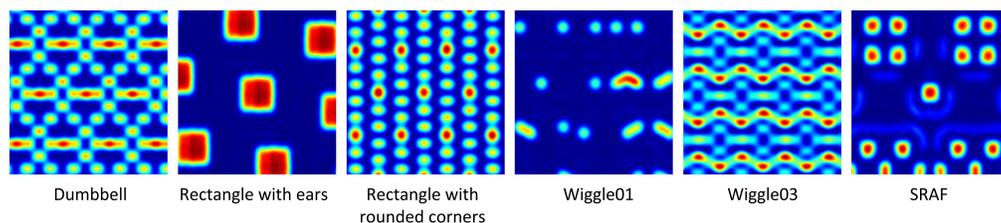
Fig. 28 Aerial images of test patterns by EUV AIMS tool.

Pattern with SRAF   (QB 0.1nm) - OASIS   (QB 2nm) - OASIS
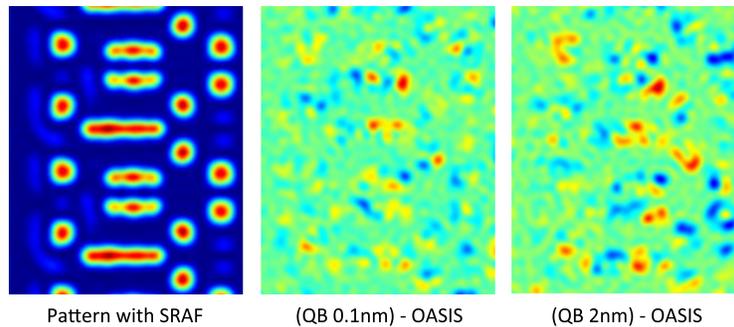
Fig. 29 Comparison of AIMS image difference to baseline for two fitting tolerance levels.

7 Observations and Future Work

Multiple options for data volume reduction were tried in this study. The classic methods of reducing vertex count still hold merit. They provide about 3.1× overall file size reduction with 1-nm deviation tolerance. However, these techniques cannot be used directly as they suffer with issues such as polygons becoming smaller in convex regions and larger in concave regions, so they cannot be adopted directly without further fine tuning. Also, simple reduction of vertices leads to issues such as losing smoothness of polygons in certain regions (as shown in Fig. 8). Downstream tools such as OPC and MPC verification might struggle to provide good solutions in such regions.

Bezier and B-spline curves were also evaluated to see how much file size reduction can be achieved. There are many reasons to choose B-splines and Beziers for this conversion and data reduction effort. These are classic curve formats with wide acceptance and popularity in other fields of CAD and computer graphics. These curves have some superior geometric properties (such as affine transform invariant, convex hull properties, etc.) that make them well suited in the semiconductor manufacturing domain. These properties can be leveraged in implementing some of the classic computational geometry solutions in the post-tapeout domain.

These formats provide improvements of 3.8× (Bezier) and 2.8× (B-spline), respectively. However, these are preliminary results and there is definitely large scope of improving file size using these techniques. Several adjustments to control point placement and parameterization changes are being worked upon, and the results of the same will be shared in future work. Also, it is clear that more focus is needed in B-spline formats for their inherent ability to provide better results in terms of curve continuity. There is also some evidence that if the ILT OPC shapes natively represent quadratic curves (such as ellipse, circles, etc.), then the compaction achieved with these curve types is far superior to any other technique. That opens up avenues of innovation for OPC and MPC tool makers to leverage these features of data exchange formats.

A similar idea tried out here was to store just the center-line (or path) for SRAFs whose width is constant and corners also made of the same radius semicircles. This again opens up opportunities for OPC tool makers to use such SRAFs and help reduce data volume and burden on downstream tools.

Preliminary investigation of changes to wafer and mask images was done, which by and large showed that the images do not deteriorate by much. All these results show that this is a good path forward for the industry to explore further and ensure that we arrive at the best format for curvilinear designs in the post-tapeout flow.

Managing data volume for full-layout curvilinear OPC is a significant challenge now that multibeam mask writers are available to produce complex curvilinear masks with reasonable write times. Various approaches to curvilinear data compaction have been examined with average compaction of 2× to 8× across a wide range of pattern shapes. It may be possible to achieve further compaction if OPC tools can utilize patterns easily represented by B-splines. Mask metrology confirms that mask EPE impact is limited to about 1 nm with conversion error tolerances of up to 2 nm. The CBF approach improves MPC cycle time by as much as 35%. A roadmap for implementation is proposed. In the near future, we hope to improve B-spline compaction,

confirm wafer process windows, and continuing to work with the EDA and user community to develop consensus on approach and standards for new formats.

Mask metrology confirms that mask EPE impact is limited to about 10% relative to baseline using conversion error tolerances of up to 2 nm. The CBF approach can improve MPC cycle time by as much as 35%. AIMS measurements suggest that while some combinations of curvilinear patterns, fitting approaches, and tolerances result in equivalent AIMS images, some do not, which suggests the need for improved data and mask metrology methods for curvilinear data.

Acknowledgments

References

1. C. Klein and E. Platzgummer, "MBMW-101: World's 1st high-throughput multi-beam mask writer," *Proc. SPIE* **9985**, 998505 (2016).
2. H. Matsumoto et al., "Multi-beam mask writer MBM-1000," *Proc. SPIE* **11518**, 115180A (2020).
3. J. Choi et al., "Requirements of data technology for EUV photomask," *Proc. SPIE* **11148**, 111480F (2019).
4. M. Fernandez Guasti and M. De La Cruz Heredia, "Diffraction pattern of a circle/square aperture," *J. Mod. Opt.* **40**(6), 1073–1080 (1993).
5. C. A. Mack et al., "Lithography performance of contact holes: II. Simulation of the effects of reticle corner rounding on wafer print performance," *Proc. SPIE* **4066**, 172–179 (2000).
6. D. S. Abrams and L. Pang, "Fast inverse lithography technology," *Proc. SPIE* **6154**, 61541J (2006).
7. B.-G. Kim et al., "Trade-off between inverse lithography mask complexity and lithographic performance," *Proc. SPIE* **7379**, 73791M (2009).
8. E. Platzgummer, C. Klein, and H. Loeschner, "Electron multi-beam technology for mask and wafer writing at 0.1 nm address grid," *Proc. SPIE* **8680**, 868004 (2013).
9. P. Rai-Choudhury, *Handbook of Microlithography and Microfabrication* (1997).
10. D. R. Herriott et al., "EBES: a practical electron lithographic system," *IEEE Trans. Electron Devices* **22**(7), 385–392 (1975).
11. J. Freyer and K. Standiford, "Design of an accurate production e-beam system," *Solid State Technol.*, 165–170 (1983).
12. P. A. Warkentin and J. A. Schoeffel, "Scanning laser technology applied to high speed reticle writing," *Proc. SPIE* **0633**, 286 (1986).
13. T. Sandstrom et al., "Sigma7100: a new architecture for laser pattern generators for 130 nm and beyond," *Proc. SPIE* **4409**, 1–7 (2001).
14. H. Matsumoto et al., "Multi-beam mask writer MBM-1000 and its application field," *Proc. SPIE* **9984**, 998405 (2016).
15. A. J. Reich, K. H. Nakagawa, and R. E. Boone, "OASIS vs. GDSII stream format efficiency," *Proc. SPIE* **5256**, 1–11 (2003).
16. P. LaCour et al., "New stream format: progress report on containing data size explosion," *Proc. SPIE* **5042**, 214 (2003).
17. S. F. Schulze, K. H. Nakagawa, and P. D. Buck, "OASIS: progress on implementing the new stream format for containing data size explosion," *Proc. SPIE* **5504**, 53–59 (2004).
18. M. Visvalingam and J. D. Whyatt, "Line generalisation by repeated elimination of points," *Cartogr. J.* **30**(1), 46–51 (1993).
19. E. V. Shikin and A. I. Plis, *Handbook on Splines for the User*, p. 96, CRC Press (1995).

20. C. De Boor, *A Practical Guide to Splines*, Revised ed., pp. 89–91, Springer-Verlag, New York (2001).

21. S. Gharat et al., "A study on various curvilinear data representations and their impact on mask manufacturing flow," *Proc. SPIE* **11613**, 116130B (2021).

22. J. Choi et al., "Curvilinear data format working group for MBMW era," *Proc. SPIE* **11610**, 116100S (2021).

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